Use the excel file accompanying Lesson 26 to generate the data in the table below – make sure to use the “second order” tab. When complete, plot the data in the empty graph at right to build the phase and magnitude plots.

|  |  |  |
| --- | --- | --- |
| FrequencyCell B2 | GainCell P10 | PhaseCell P9 |
| 100 |  |  |
| 300 |  |  |
| 500 |  |  |
| 1,000 |  |  |
| 1,300 |  |  |
| 1,500 |  |  |
| 3,000 |  |  |
| 5,000 |  |  |
| 7,000 |  |  |
| 10,000 |  |  |
| 13,000 |  |  |
| 15,000 |  |  |



Calculate the slope of the Gain (to the right of the cut-off

frequency). Show your work here:

Use the equations presented in class to generate the coefficients

for a 2nd order low pass filter with a cut-off frequency of 300Hz.

|  |  |  |
| --- | --- | --- |
| Coefficient | Decimal | Fixed Point |
| X[n-2] |  |  |
| X[n-1] |  |  |
| X[n-0] |  |  |
| Y[n-1] |  |  |
| Y[n-2] |  |  |

Build a project around the VHDL code for this lesson. Plug the coefficients for your filter above into the right channel filter. Synthesize your design, download and listen to the difference between the left and right audio channels.

-------------------------------------------------------------------------------------

Audio\_Codec : Audio\_Codec\_Wrapper

 Port map ( clk => clk,

 reset\_n => reset\_n,

 ac\_mclk => ac\_mclk,

 ac\_adc\_sdata => ac\_adc\_sdata,

 ac\_dac\_sdata => ac\_dac\_sdata,

 ac\_bclk => ac\_bclk,

 ac\_lrclk => ac\_lrclk,

 ready => ready,

 L\_bus\_in => LdacValue, -- left channel input to DAC

 R\_bus\_in => RdacValue, -- right channel input to DAC

 L\_bus\_out => LadcValue, -- left channel output from ADC

 R\_bus\_out => RadcValue, -- right channel output from ADC

 scl => scl,

 sda => sda);

 left\_filter\_lpf1000: entity work.IIR\_Biquad(arch)

 -- low pass 2nd order butterworth fl = 1000Hz, Fs = 48000Hz

 -- http://www.earlevel.com/main/2013/10/13/biquad-calculator-v2/

 generic map(Coef\_b0 => B"00\_00\_0000\_0100\_0000\_0010\_1001\_0110\_1101", -- +0.003916127

 Coef\_b1 => B"00\_00\_0000\_1000\_0000\_0101\_0010\_1101\_1010", -- +0.007832253

 Coef\_b2 => B"00\_00\_0000\_0100\_0000\_0010\_1001\_0110\_1101", -- +0.003916127

 Coef\_a1 => B"10\_00\_1011\_1101\_0001\_0111\_0011\_1010\_0010", -- -1.815341083

 Coef\_a2 => B"00\_11\_0101\_0010\_1111\_0011\_0010\_0001\_0001") -- +0.831005589

 port map ( clk => clk,

 n\_reset => reset,

 sample\_trig => ready,

 X\_in => LadcValue,

 filter\_done => OPEN,

 Y\_out => L\_filter\_lpf1000);

 process (clk)

 begin

 if (rising\_edge(clk)) then

 if reset = '0' then

 LdacValue <= (others => '0'); RdacValue <= (others => '0');

 elsif(ready = '1') then

 if (filter\_switch = "00") then

 LdacValue <= LadcValue; RdacValue <= RadcValue;

 else

 LdacValue <= L\_filter\_lpf1000; RdacValue <= R\_filter\_lpf1000;

 end if;

 end if;

 end if;

 end process;