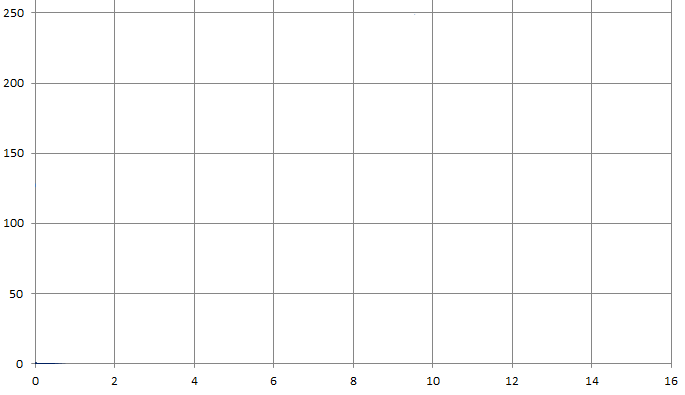
Use the sinusoidal lookup table at left to generate a sine wave using a Q4.4 format phase increment of 0001.1011. Plot the “Base” and “Base + Offset\*Delta” columns in the graph below.

|  |  |
| --- | --- |
| 0 | 127 |
| 1 | 175 |
| 2 | 216 |
| 3 | 244 |
| 4 | 253 |
| 5 | 244 |
| 6 | 216 |
| 7 | 175 |
| 8 | 127 |
| 9 | 78 |
| 10 | 37 |
| 11 | 9 |
| 12 | 0 |
| 13 | 9 |
| 14 | 36 |
| 15 | 78 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Time | Index | Base | Delta | Offset\*Delta | Base + Offset\*Delta |
| 0 | 0000.0000 | 127 | 175-127 = 48 = 110000 | 0.0000\*110000 = 00000.0000 | 127+0 = 127 |
| 1 | 0001.1011 | 175 | 216-175 = 41 = 101001 | 0.1011\*101001 = 11100.0011 | 175+28 = 203 |
| 2 |  |  |  |  |  |
| 3 |  |  |  |  |  |
| 4 |  |  |  |  |  |
| 5 |  |  |  |  |  |
| 6 |  |  |  |  |  |
| 7 |  |  |  |  |  |
| 8 |  |  |  |  |  |
| 9 |  |  |  |  |  |
| 10 |  |  |  |  |  |
| 11 |  |  |  |  |  |
| 12 |  |  |  |  |  |
| 13 |  |  |  |  |  |
| 14 |  |  |  |  |  |



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-- BRAM\_SDP\_MACRO: Simple Dual Port RAM 7 Series

-- Source: Xilinx HDL Libraries Guide, version 2012.4

-- Link: https://www.xilinx.com/support/documentation/sw\_manuals/xilinx2012\_2/ug953-vivado-7series-libraries.pdf

-- Page: 10

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sampleMemory: BRAM\_SDP\_MACRO

generic map (

BRAM\_SIZE => "18Kb", -- Target BRAM, "18Kb" or "36Kb"

DEVICE => "7SERIES", -- Target device: "VIRTEX5", "VIRTEX6", "SPARTAN6", "7SERIES"

DO\_REG => 0, -- Optional output register disabled

INIT => X"000000000000000000", -- Initial values on output port

INIT\_FILE => "NONE", --

WRITE\_WIDTH => 16, -- Valid values are 1-72 (37-72 only valid when BRAM\_SIZE="36Kb")

READ\_WIDTH => 16, -- Valid values are 1-72 (37-72 only valid when BRAM\_SIZE="36Kb")

SIM\_COLLISION\_CHECK => "NONE", -- Simulation collision check

SRVAL => X"000000000000000000", -- Set/Reset value for port output

INIT\_00 => X"8BC28AF98A31896988A087D8870F8647857E84B583EC8323825A819180C88000",

INIT\_01 => X"9830976A96A595DF95199452938C92C591FE913790708FA98EE18E198D528C8A",

INIT\_02 => X"A462A3A2A2E0A21FA15DA09B9FD89F169E529D8F9CCB9C079B439A7F99BA98F5",

INIT\_3E => X"7247717F70B76FF06F296E616D9A6CD46C0D6B476A8069BA68F5682F676A66A5",

INIT\_3F => X"7ECF7E067D3D7C747BAC7AE37A1A7951788977C076F7762F7567749F73D6730E")

port map (

DO => DO, -- Output read data port, width defined by READ\_WIDTH parameter

RDADDR => vecAddrRead, -- Input address, width defined by port depth

RDCLK => clk, -- 1-bit input clock

RST => reset, -- active high reset

RDEN => '1', -- read enable

REGCE => '1', -- 1-bit input read output register enable - ignored

DI => DI, -- Dummy write data - never used in this application

WE => "00", -- write to neither byte

WRADDR => "0000000000", -- Dummy place holder address

WRCLK => clk, -- 1-bit input write clock

WREN => '0'); -- we are not writing to this RAM