Hardware Block Diagram of a Nios II Processor Custom Instruction

Optional interface to external memory, FIFO, or other logic

dataa[31..0] → Combinatorial → result[31..0]

datab[31..0] →

clk →
clk_en →   Multi-cycle → done
reset →
start →

n[7..0] → Extended

a[4..0] →
readra →
b[4..0] →   Internal Register File
readrb →
c[4..0] →
writerc →