Homework 2: Binary Round Up System

The goal of this assignment is to build a combinational system that rounds up a given n-bit binary data to its next higher binary data (2^N). See example below for clarification.

input	output
12	16
24	32
513	1,024
4,096	4,096 (same as input)

Notice that the system will need n+1-bit output for an n-bit input.

Specification:

The circuit must be combinational (no clock). The design should take an unsigned 16-bit input (ranges from 0 to 65,535) and generate a 16-bit output with one overflow bit (bit n+1). As a suggestion, you should consider building a one bit cell that can be used to perform round up. The final implementation is to use 16 of cells to make a 16-bit circuit.

Deliverables:

Basic Design (**due: see course web-page**): Two high level designs:

1. A design describing the input/output signals of a basic cell. It is OK if you need to add extraneous signals to help initialize the circuit and propagate information.
2. A design describing the interconnection among the 16 basic cells.

Implementation (**due: see course web-page**): The implementation in VHDL. Three files will be needed:

1. A VHDL files describing the basic cells.
2. A VHDL file representing the final design.
3. A waveform simulation file used to validate the correctness. There should be at least 25 test cases on this file. Identify some interesting test cases that can cause the system to fail.

Final report (**due: see course web-page**): The report should contain the following information:

1. The amount of time spent on the assignment.
   - How much time spent learning the VHDL?
   - How much time spent in the design phase?
   - How much time spent in the refinement of the design (after February 6th)?
   - How much time spent in the implementation?
2. The difficulties encountered.
3. The level of difficult of the assignment (0 means easy; 10 means impossible to do).
4. Resource usage and timing analysis.

All submissions must be made through your hand-in account.