Homework 2: Virtual Memory and Schduling

Due date: Check the class website.

1. Consider paged virtual memory systems. Assume a page size of 512 bytes (2^9), and that processes in this system can have a maximum virtual address space of 64K bytes (2^{16}). The system is currently configured with 5K bytes of physical memory.

i) How many frames are in the physical address space?

ii) How many pages are in the virtual address space?

iii) A user process generates the virtual address 14,359 (11100000010111 in binary). Explain how the system establishes the corresponding physical address assuming that the hardware MMU is used.

2. Now consider a paged virtual memory system with only 5 page frames. Assume the execution of a program generates the following address trace

a b c d e e c f d b a e c e

where *a*, *b*, *c*, *d*, *e*, and *f*, are the pages that are referenced and the page frames are initially empty.

i) How many page faults occur with FIFO Page Replacement?

(You may use the table below to help you in computing the number of faults and to receive partial credit if you get the wrong answer.)

Time	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Request	*a*	*b*	*c*	*d*	*E*	*E*	*c*	*f*	*d*	*b*	*a*	*e*	*c*	*e*
Frame 0														
Frame 1														
Frame 2														
Frame 3														
Frame 4														
Fault?														

ii) How many page faults occur with LRU Page Replacement?

(You may use the table below to help you in computing the number of faults and to receive partial credit if you get the wrong answer.)

Time	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Request	*a*	*b*	*c*	*d*	*e*	*e*	*c*	*f*	*d*	*b*	*a*	*e*	*c*	*e*
Frame 0														
Frame 1														
Frame 2														
Frame 3														
Frame 4														
Fault?														

3. Consider a computer with a paged logical address space, composed of 32 pages of 2 Kbytes each, that is mapped into a 1-Mbyte physical memory space.

a) What is the format of the processor's logical address? That is, show how many bits are used in the logical address and how they are used.

b) What is the length and width of the page table (i.e., number of entries and number of bits per entry)?

4. Consider the following set of processes, with the length of the CPU-burst time given in milliseconds

Process	Burst-time	Priority
P1	9	3
P2	1	1
P3	2	3
P4	1	4
P5	6	2

Processes are assumed to have arrived in the order P1, P2, P3, P4, P5, all at time 0.
a) What is the turnaround time of each process for using the following scheduling algorithms?

i) FCFS

ii) Round robin with 1 ms quantum

iii) Shortest process next

iv) Non-preemptive priority scheduling (use FCFS in case of equal priority). Assume lower value means higher priority.

b) What is the average waiting time (over all processes) for each of the scheduling algorithms in part a?