

## Journal Publications

Chen, Z., Seth, S., Xiong, D. and Bhattacharya, B. B. 2010. PVT: Unified Reduction of Test Power, Volume, and Test Time using Double-Tree Scan Architecture. *Journal of Low Power Electronics (JOLPE)*, 6, 3, 457-468. [http://www.aspbs.com/jolpe/contents\\_jolpe2010.htm#v6n3](http://www.aspbs.com/jolpe/contents_jolpe2010.htm#v6n3)

Nagy, G., Seth, S. and Viswanathan, M. 2009. Projection methods require black border removal. *IEEE Transactions on PAMI*, 31, 4, 762-762. <http://csdl2.computer.org/comp/trans/tp/5555/01/tp2008990430.pdf>

Saha, I., Bhattacharya, B. B., Zhang, S. and Seth, S. C. 2008. Planar Straight-Line Embedding of Double-Tree Scan Architecture on a Rectangular Grid. *Fundamenta Informaticae*, 89, 2, 331-344. <http://fi.mimuw.edu.pl/>

Samal, A., Seth, S. C. and Cueto, K. 2004. A Feature-Based Approach to Conflation of Geospatial Sources. *Int. Journal of Geographic Information Science*, 18, 5, 459-489. [http://pdfserve.informaworld.com/604833\\_731197584\\_713599861.pdf](http://pdfserve.informaworld.com/604833_731197584_713599861.pdf)

Cui, H., Seth, S. C. and Mehta, S. K. 2003. Modeling Fault Coverage of Random Test Patterns. *Journal of Electronic Testing: Theory & Applications (JETTA)*, 19, 3, 271-284.

Li, L., Nagy, G., Samal, A., Seth, S. and Xu, Y. 2000. Integrated Text and Line Extraction from a Topographic Map. *Int Jour. Document Analysis and Recognition (IJ DAR)*, Springer, 2, 4, 177-185.

Einspahr, K., Mehta, S. K. and Seth, S. C. 1999. A Synthesis for Testability Scheme for Finite State Machine Using Clock Control. *IEEE Trans Computer Aided Design*, 18, 12, 1780-1792.

Yu, Y., Samal, A. and Seth, S. 1997. A system for Recognizing a Large Class of Engineering Drawing. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, 19, 8, 868-890.

Einspahr, K. and Seth, S. C. 1995. A Switch-Level Test Generation System for Synchronous and Asynchronous Circuits. *Journal of Electronic Testing: Theory and Applications (JETTA)*, 6, 1, 59-73.

Kenyon, P., Seth, S., Agrawal, P., Clematis, A., Doderio, G. and Gianuzzi, V. 1995. Programming Pipelined CAD Applications on Message Passing Architectures. *Concurrency Practice and Experience*, 7, 4, 315-337.

Yu, Y., Samal, A. and Seth, S. 1994. Isolating Symbols from Connection Lines in a Class of Engineering Drawings. *Pattern Recognition*, 27, 3, 391-404.

Agrawal, P., Agrawal, V. D. and Seth, S. C. 1993. A new method for generating tests for delay faults in non-scan circuits. *IEEE Design & Test of Computers*, 10, 1, 20-28.

Das, D. V., Seth, S. and Agrawal, V. D. 1993. Accurate Computation of Field Reject Ratio Based on Fault Latency. *IEEE Trans. on VLSI Systems*, 1, 4, 537-545.

Krishnamoorthy, M., Nagy, G., Seth, S. and Viswanathan, M. 1993. Syntactic segmentation and labeling of digitized pages from technical journals. *IEEE Transaction on Pattern Analysis and Machine Intelligence*, 15, 7, 737-747.

Krishnamoorthy, M., Molholt, P., Nagy, G., Seth, S. and Viswanathan, M. 1993. Tools for Document Image Utility. *Library Hi Tech*, 11, 3, 73-92.

Nagy, G., Seth, S. and Viswanathan, M. 1992. A prototype document image analysis system for technical journals. *IEEE Computer*, 25, 7, 10-22.

- Seth, S. C., Agrawal, V. D. and Farhat, H. 1990. A statistical theory of digital circuit testability. *IEEE Trans. Computers*, 38, 11, 582-586.
- Seth, S. C. and Agrawal, V. D. 1989. A new model for computation of probabilistic testability in combinational circuits. *Integration, the VLSI Journal*, 7, 1, 49-75.
- Bhattacharya, B. B. and Seth, S. C. 1989. Design of parity testable combinational circuits. *IEEE Transactions on Computers*, 38, 11, 1580-1584.
- Lipsky, L. L. and Seth, S. C. 1989. Signal probabilities in And-Or trees. *IEEE Transactions on Computers*, 38, 11, 1558-1563.
- Nagy, G., Seth, S. and Einspahr, K. 1987. Decoding substitution ciphers by means of word matching with application to OCR. *IEEE Trans. Pattern Analysis and Machine Intelligence*, 9, 5, 710-715.
- Seth, S. C. and Agrawal, V. D. 1985. A review of testing of digital devices. Invited review. *IETE Technical Review, The Institute of Electronics and Telecommunications Engineers, India*, 2, 11, 363-374.
- Seth, S. C. and Agrawal, V. D. 1985. Cutting Chip Testing Costs. *IEEE Spectrum*, 22, 4, 38-45.
- Seth, S. C. and Agrawal, V. D. 1984. Characterizing the LSI yield equation from chip test data. *IEEE Trans. Computer-Aided Design*, 3, 4, 123-126.
- Hsiao, T.-C. and Seth, S. C. 1984. The use of Rademacher-Walsh spectrum in random compact testing. *IEEE Transactions on Computers*, 33, 10, 934-937.
- Seth, S. C. and Lipsky, L. L. 1983. A simplified method to calculate failure times in fault-tolerant systems. *IEEE Transactions on Computer*, 32, 8, 754-756.
- Agrawal, V. D., Seth, S. C. and Agrawal, P. 1982. Fault coverage requirements in production testing of LSI circuits. *IEEE Solid State Circuit Journal*, 0, 0, 57-61.
- Seth, S. C. and Narayanaswamy, K. 1981. A graph model for pattern-sensitive faults in random access memories. *IEEE Trans. on Computers*, 30, 12, 973-977.
- Seth, S. C. and Agrawal, V. D. 1981. Forecasting field-reject rate of LSI chips. *IEEE Electronic Device Letters*, 0, 11, 286-287.
- Kodandapani, K. L. and Seth, S. C. 1978. On combinational networks with restricted fanout. *IEEE Trans. on Computers*, 27, 4, 309-318.
- Seth, S. C. 1977. Data compression techniques in logic testing: An extension of transition counts. *Journal of Design Automation and Fault Tolerant Computing*, 1, 2, 90-114.
- Seth, S. C. and Kodandapani, K. L. 1977. Diagnosis of faults in linear tree networks. *IEEE Trans. on Computers*, 26, 1, 29-33.
- Steckelberg, J. M. and Seth, S. C. 1977. On a relation between algebraic programs and Turing machines. *Information Processing Letters*, 6, 0, 180-183.

### **Conference Publications**

- Jin, D. and Seth, S. 2012. A Lexical Approach on Building Category Parse Trees for Web Tables . In Proceedings of the *National Conference on Undergraduate Research (NCUR 2012)*, Ogden, Utah, 1. [Accepted]
- Jiang, D. Z. H. and Seth, S. 2012. Locality & Utility Co-optimization for Practical Capacity Management of Shared Last Level Caches. In Proceedings of the *International Conference on Supercomputing*, Venice, Italy, 2012, 1-10. [Accepted]
- Nagy, G., Seth, S., Jin, D., Embley, D., Machado, S. and Krishnamoorthy, M. S. 2011. Data Extraction from Web Tables: the Devil is in the Details. In Proceedings of the *11th Int. Conf. Document Analysis and Recognition, 2011*, Beijing, China, 242-246.
- Embley, D. E., Krishnamoorthy, M., Nagy, G. and Seth, S. 2011. Factoring Web Tables. In Proceedings of the *24th International Conference on Industrial, Engineering & Other Applications of Applied Intelligent Systems, K. G. Mehrotra et al. (Eds.): IEA/AIE 2011, Part I, LNAI 6703*, Syracuse, 253-263.  
<http://www.lcs.syr.edu/iea-aie2011/>
- Chen, Z., Seth, S., Xiong, D. and Bhattacharya, B. B. 2011. Scan Chain Diagnosis in the Presence of System Logic Faults. In Proceedings of the *20th Asian Test Symposium, Nov 21-23, 2011*, New Delhi, India, 297-302.
- Chen, Z., Seth, S. and Xiang, D. 2010. A Novel Hybrid Delay Testing Scheme with Low Test Power, Volume, and Time. In Proceedings of the *VLSI Test Symposium*, 4, Santa Clara, CA, 2010, 307-312.  
<http://0-ieeeexplore.ieee.org.library.unl.edu/stamp/stamp.jsp?tp=&arnumber=5469547>
- Seth, S. C., Chen, Z., Xiang, D. and Bhattacharya, B. B. 2010. A Unified Solution to Scan Test Volume, Time, and Power Minimization. In Proceedings of the *International Conference on VLSI Design*, 1, Bangalore, India, 2010, 1-6. <http://0-ieeeexplore.ieee.org.library.unl.edu/stamp/stamp.jsp?tp=&arnumber=5401360>
- Seth, S., Jandhyala, R., Krishnamoorthy, M. and Nagy, G. 2010. Analysis and Taxonomy of Column Header Categories for Web Tables . In Proceedings of the *9th IAPR Workshop on Document Analysis and Systems (DAS 2010)*, Cambridge, MA, 1-8.  
[http://www.cubs.buffalo.edu/DAS2010/DAS2010\\_CFP\\_Ver6b.pdf](http://www.cubs.buffalo.edu/DAS2010/DAS2010_CFP_Ver6b.pdf)
- Zhan, D., Jiang, H. and Seth, S. C. 2010. Exploiting Set-Level Non-Uniformity of Capacity Demand to Enhance CMP Cooperative Caching. In Proceedings of the *International Parallel & Distributed Processing Symposium (IPDPS 2010)*, Atlanta, Georgia. <http://ponca.unl.edu/facdb/csefacdb/TechReportArchive/TR-UNL-CSE-2009-0013.pdf>
- Schemm, N., Balkir, S. and Seth, S. 2010. Hardware Implementation of the Double-Tree Scan Architecture. In Proceedings of the *International Symposium on Circuits and Systems (ISCAS)*, Paris, France, 2010, 429-432. <http://0-ieeeexplore.ieee.org.library.unl.edu/stamp/stamp.jsp?tp=&arnumber=5537687>
- Zhan, D., Jiang, H. and Seth, S. 2010. STEM: Spatiotemporal Management of Capacity for Intra-Core Last Level Caches. In Proceedings of the *43rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-43) (Acceptance: 18%)*, Atlanta, GA, 2010, 163-174.  
<http://cse.unl.edu/~seth/pubs/STEM-MICRO2010.pdf>
- Nagy, G., Seth, S., Silversmith, W., Krishnamoorthy, M., Jandhyala, R. C. and Padmanabhan, R. 2009. From isothetic tessellations to web tables. In Proceedings of the *Mathematical Knowledge Management 2009*, Grand Bend, Ontario, Canada.  
[/facdb/csefacdb/ConferencePubArchive/seth200903181445mkm09\\_submission\\_24.pdf](http://facdb/csefacdb/ConferencePubArchive/seth200903181445mkm09_submission_24.pdf)
- Padmanabhan, R., Jandhyala, R. C., Krishnamoorthy, M., Nagy, G., Silversmith, W. and Seth, S. 2009. How many different kinds of tables are there?. In Proceedings of the *8th IAPR Workshop on Graphics*

*Recognition (GREC 2009)*, La Rochelle, France. <http://0-springerlink.com.library.unl.edu/content/r77k22454768570m/fulltext.pdf>

Kang, J., Seth, S., Chang, Y.-S. and Gangaram, V. 2008. Efficient Selection of Observation Points for Functional Tests. In Proceedings of the *9th International Symposium on Quality Electronic Design (ISQED 2008)*, San Jose, California, 236-241. <http://0-ieeexplore.ieee.org.library.unl.edu/stamp/stamp.jsp?tp=&arnumber=4479732>

Kang, J., Seth, S. C. and Gangaram, V. 2007. Efficient RTL Coverage Metric for Functional Test Selection. In Proceedings of the *25th IEEE VLSI Test Symposium*, Berkeley, CA, 2007, 318-324. <http://0-ieeexplore.ieee.org.library.unl.edu/stamp/stamp.jsp?tp=&arnumber=4209931>

Kang, J., Seth, S. C. and Mehta, S. K. 2007. Symbolic Path Sensitization Analysis and Applications. In Proceedings of the *16th Asian Test Symposium (ATS '07)*, Beijing, China, 2007, 439-444. <http://0-ieeexplore.ieee.org.library.unl.edu/stamp/stamp.jsp?tp=&arnumber=4388051>

Joshi, A., Nagy, G., Lopresti, D. and Seth, S. C. 2006. A Maximum-Likelihood Approach to Symbolic Indirect Correlation. In Proceedings of the *International Conference on Pattern Recognition*, Hong Kong, China, 2006, 99-103.

Lopresti, D., Nagy, G., Seth, S. and Zhang, X. 2006. Multi-Character Field Recognition for Arabic and Chinese Handwriting. In Proceedings of the *Summit on Arabic and Chinese Handwriting (SACH06)*, College Park, Maryland, 2006, 93-100.

Zhang, S., Seth, S. C. and Bhattacharya, B. B. 2005. Efficient test compaction for pseudo-random testing. In Proceedings of the *Asian Test Symposium (ATS05)*, Calcutta, India, 2005, 337-342.

Zhang, S., Seth, S. C. and Bhattacharya, B. B. 2005. On Finding Consecutive Test Vectors in a Random Sequence for Energy-Aware BIST Design. In Proceedings of the *18th Int. Conf. on VLSI Design*, Calcutta, India, 2005, 491-496.

Lin, L., Samal, A. and Seth, S. 2004. Context Directed Interpretation of Remotely Sensed Urban Images. In Proceedings of the *ASPRS 2004 Fall Conference*, Kansas City, 1-9.

Nagy, G., Lopresti, D., Krishnamoorthy, M., Lin, Y., Mehta, S. and Seth, S. 2004. Nonparametric Classifier for Unsegmented Text. In Proceedings of the *Document Recognition and Retrieval XI (part of IS&T/SPIE Int. Symposium on Electronic Imaging 2004)*, 5296, San Jose, CA, 1-7.

Bhattacharya, B. B., Seth, S. C. and Zhang, S. 2003. Double-Tree Scan: A Novel Low-Power Scan-Path Architecture. In Proceedings of the *International Test Conference*, Baltimore, 2003, 470-479.

Nagy, G., Seth, S. C., Mehta, S. K. and Lin, Y. 2003. Indirect Symbolic Correlation Approach to Unsegmented Text Recognition. In Proceedings of the *DIAR03: Workshop on Document Image Analysis and Retrieval (in conjunction with CVPR'03)*, available through *IEEE Digital Library*, 3, Madison, WI, 2003, 22-32.

Bhattacharya, B. B., Seth, S. C. and Zhang, S. 2003. Low-Energy BIST Design for Scan-Based Logic Circuits. In Proceedings of the *16th Int Conference on VLSI Design*, New Delhi, 2003, 546-551.

Cui, H. and Seth, S. 2002. A Novel method to improve the test efficiency of VLSI tests. In Proceedings of the *15th International Conference on VLSI Design (ASP-DAC/VLSI Design 2002)*, 499-504.

Scott, Q-F. L.. S. and Seth, S. C. 2001. A machine learning framework for automatically annotating web pages with simple HTML ontology extension (SHOE). In Proceedings of the *International Conference on Intelligent Agents, Web Technology and Internet Commerce (IAWTIC'2001)*, Las Vegas, NV, 303-310.

- Sylwester, D. and Seth, S. 2001. Adaptive segmentation of document images. In Proceedings of the *6th International Conference on Document Analysis and Recognition – ICDAR 2001*, Seattle, 827-831.
- Weiss, M. W., Seth, S. C., Mehta, S. K. and Einspahr, K. L. 2001. Design Verification and Functional Testing of Finite State Machines. In Proceedings of the *International Conference on VLSI Design – VLSI Design 2001*, Bangalore, India, 189-195.
- Samal, A., Seth, S. and Cueto, K. 2001. Like-Feature Detection in Geo-Spatial Sources. In Proceedings of the *SPIE: Geo-Spatial Image and Data Exploitation II, William E. Roper; Ed.*, 4383, Orlando, Florida, 2001, 62-73.
- Nagy, G. and Seth, S. 2001. Twenty questions for document classification (Invited presentation). In Proceedings of the *Document Layout Interpretation and its Applications Workshop*, Seattle, 2001, 1-3.
- Cueto, K., Samal, A. and Seth, S. 2000. Context-based similarity for GIS feature matching. In Proceedings of the *GIScience 2000*, Savannah, Georgia, USA, 1.
- Weiss, M. W., Seth, S. C., Mehta, S. K. and Einspahr, K. L. 2000. Exploiting Don't Cares to Enhance Functional Tests. In Proceedings of the *International Test Conference*, Atlantic City, NJ, 2000, 538-546.
- Mehta, S. K. and Seth, S. C. 1999. "Empirical Computation of Reject Ration in VLSI Testing". In Proceedings of the *International Conference on VLSI Design*, Goa India, 1999, 506-511.
- Li, L., Nagy, G., Samal, A., Seth, S. and Xu, Y. 1999. Cooperative Text and Line-Art Extraction from a Topographic Map. In Proceedings of the *International Conf on Document Image Analysis and Recognition(ICDAR)*, Bangalore, India, 1999, 467-470.
- McCoy, P. T., Seth, S. C., Reichenbach, S. E. and Samal, A. 1998. "Digital Camera Traffic Accident Investigation System". In Proceedings of the *1998 Transportation Conference Proceedings, Crossroads 2000*, Iowa State University, Ames, Iowa, 159-163.
- Agrawal, V. D. and Seth, S. 1998. "Mutually Disjoint Signals and Probability Calculation in Digital Circuits". In Proceedings of the *Eight Great Lakes Symposium on VLSI*, Lafayette, Louisiana, 1998, 307-312.
- Einspahr, K. L., Mehta, S. K. and Seth, S. C. 1998. "Synthesis of Sequential Circuits with Clock Control to Improve Testability". In Proceedings of the *Seventh Asian Test Symposium*, Singapore, 1998, 472-477.
- Nagy, G., Samal, A., Seth, S., Fisher, T., Guthmann, E., Kalafala, K., Li, L., Sarkar, P., Sivasubramaniam, S. and Xu, Y. 1997. "A Prototype for Adaptive Association of Street Names with Streets on Maps". In Proceedings of the *Second IAPR Workshop on Graphics Recognition (GREC 97)*, 1997, 268.
- Nagy, G., Samal, A., Seth, S., Fisher, T., Guthmann, E., Kalafala, K., Li, L., Sivasubramaniam, S. and Xu, Y. 1997. "Reading Street Names from Maps -- Technical Challenge". In Proceedings of the *GIS/LIS Conference*, Cincinnati, Ohio, 1997, 89-97.
- Mehta, S. K., Seth, S. C. and Einspahr, K. L. 1997. Synthesis for Testability by Two-Clock Control. In Proceedings of the *10-th International Conference on VLSI Design*, Hyderabad, India, 1997, 279-283.
- Mehta, S. K., Seth, S. and Einspahr, K. L. 1996. A New Synthesis for Testability Scheme Using Two-Clock Control. In Proceedings of the *3rd Int Test Synthesis Workshop, Santa Barbara (presentation only, no printed proceedings)*, 1996.
- Sylwester, D. R. and Seth, S. 1996. Column Extraction from Telephone White Pages for OCR (Poster Paper). In Proceedings of the *IAPR Workshop on Document Analysis Systems*, Malvern, PA, 1996.

- Einspahr, K. L., Seth, S. C. and Agrawal, V. D. 1996. Improving Circuit Testability by Clock Control. In Proceedings of the *Sixth Great Lakes Symposium on VLSI*, Ames, Iowa, 1996, 288-293.
- Yu, Y., Samal, A. and Seth, S. C. 1995. A System for Recognizing a Large Class of Engineering Drawings. In Proceedings of the *Third Int Conf Document Analysis and Recognition (ICDAR)*, Montreal, Canada, 1995, 791-794.
- Sylwester, D. and Seth, S. 1995. A Trainable, Single-Pass Algorithm for Column Segmentation. In Proceedings of the *Third Int Conf Document Analysis and Recognition (ICDAR)*, Montreal, Canada, 1995, 615-618.
- Scott, S., Samal, A. and Seth, S. 1995. HGA: A hardware-based genetic algorithm. In Proceedings of the *Third International Symposium on Field-Programmable Gate Arrays*, Monterey, California, 1995, 53-59.
- Scott, S. D., Samal, A. and Seth, S. 1995. HGA: A Hardware-Based Genetic Algorithm. In Proceedings of the *Symposium of Field Programmable Gate Arrays*, Monterey, California, 1995, 53-59.
- Venkataraman, S., Seth, S. and Agrawal, P. 1995. Parallel Test Generation with Low Communication Overhead. In Proceedings of the *8th Int Conf VLSI Design*, New Delhi, 1995, 116-120.
- Seth, S., Gowen, L., Payne, M. and Sylwester, D. 1994. Logic Simulation using an Asynchronous Parallel Discrete- Event Simulation Model on SIMD Machine. In Proceedings of the *7th Int. Conference on VLSI Design*, 1994, 29-32.
- Yu, Y., Samal, A. and Seth, S. 1993. Automatic Segmentation of Engineering Drawings with Symbols and Connections. In Proceedings of the *Second Annual Symposium on Document Analysis and Information Retrieval*, 1993, 317-338.
- Einspahr, K. L., Seth, S. C. and Agrawal, V. D. 1993. Clock Partitioning for Testability. In Proceedings of the *Third IEEE Great Lakes Symposium on VLSI*, 1993, 42-46.
- Einspahr, K. and Seth, S. C. 1992. A switch-level test generation system. In Proceedings of the *Int. Conference on VLSI Design*, 1992, 43-48.
- Agrawal, P., Agrawal, V. D. and Seth, S. C. 1992. Dynamic timing analysis with partial scan activation in sequential circuits. In Proceedings of the *Euro-DAC/Euro-VHDL 92*, 1992, 138-141.
- Agrawal, V. D., Seth, S. C. and Deogun, J. S. 1991. Design for testability and test generation with two clocks. In Proceedings of the *Int. Conference on VLSI Design*, 1991, 112-117.
- Das, D. V., Seth, S. C. and Agrawal, V. D. 1991. Estimating the quality of manufactured digital sequential circuits. In Proceedings of the *Int. Test Conference*, 1991, 210-217.
- Sivaramakrishnan, V., Seth, S. C. and Agrawal, P. 1991. Parallel test pattern generation using boolean satisfiability. In Proceedings of the *Int. Conference on VLSI Design*, 1991, 69-74.
- Das, D. V., Seth, S. C., Wagner, P. T., Anderson, J. C. and Agrawal, V. D. 1990. An experimental study on reject ratio prediction for VLSI circuits: Kokomo revisited. In Proceedings of the *Int. Test Conference*, 1990, 712-720.
- Kenyon, P., Agrawal, P. and Seth, S. 1990. High-level microprogramming: An optimizing compiler for a processing element of a CAD accelerator. In Proceedings of the *23rd Int.Symp. and Workshop on Microprogramming and Microarchitectur*, 1990, 97-106.
- Seth, S. C., Agrawal, V. D. and Farhat, H. 1989. A theory of testability with applications to fault coverage analysis. In Proceedings of the *1st European Test Conference*, Paris, 1989, 139-143.

- Hudli, R. and Seth, S. C. 1989. Testability analysis of synchronous sequential circuits based on structural data. In Proceedings of the *Int. Test Conference*, 1989, 364-372.
- Ke, W., Seth, S. C. and Bhattacharya, B. B. 1988. A fast fault simulation algorithm for combinational circuits. In Proceedings of the *Int. Conference on Computer Aided Design*, 1988, 166-169.
- Hudli, R., Ke, W. and Seth, S. C. 1988. Structural profile of benchmark circuits relating to the test generation problem. In Proceedings of the *Second Int. Conference on VLSI Design*, 1988, 438-447.
- Agrawal, V. D., Farhat, H. and Seth, S. C. 1988. Test generation by fault sampling. In Proceedings of the *Int. Conference on Computer Design (ICCD)*, 1988, 58-61.
- Seth, S. C. 1988. What is the path to fast fault simulation? Invited panelist statement. In Proceedings of the *Int. Test Conference*, 1988, 186-188.
- Bhattacharya, B. B. and Seth, S. C. 1987. On the reconvergent structure of combinational circuits with applications to compact testing. In Proceedings of the *17th Int. Symposium. on Fault Tolerant Computing*, 1987, 264-269.
- Seth, S. C., Bhattacharya, B. B. and Agrawal, V. D. 1986. An exact analysis for efficient computation of random- pattern testability in combinational circuits. In Proceedings of the *16th Int. Symposium on Fault Tolerant Computing*, 1986, 318-323.
- Nagy, G., Seth, S., Einspahr, K. and Meyer, T. 1986. Efficient algorithms to decode substitution ciphers with applications to OCR. In Proceedings of the *8-th Int. Conference on Pattern Recognition (ICPR)*, 1986, 352-355.
- Seth, S. C. and Muralidhar, R. 1985. Analysis and design of robust data structures. In Proceedings of the *Proc Int.Fault Tolerant Computing Symposium*, 1985, 14-19.
- Seth, S. C., Pan, L. and Agrawal, V. D. 1985. PREDICT - Probabilistic Estimation of Digital Circuit Testability. In Proceedings of the *Proc Int.Fault Tolerant Computing Symposium*, 1985, 220-225.
- Seth, S. C. 1985. Predicting fault coverage from probabilistic testability. Invited contribution as a panelist. In Proceedings of the *Int. Test Conference*, 1985, 803-805.
- Agrawal, V. D. and Seth, S. C. 1985. Probabilistic testability. In Proceedings of the *Int. Conference on Computer Design*, 1985, 562-565.
- Agrawal, V. D., Seth, S. C. and Chuang, C. C. 1985. Probabilistically guided test generation. In Proceedings of the *Int. Symposium on Circuits and Systems*, 1985, 687-690.
- Nagy, G. and Seth, S. C. 1984. Hierarchical image representation with application to optically scanned documents. In Proceedings of the *7th Int. Conference on Pattern Recognition (ICPR)*, 1984, 347-349.
- Seth, S. C. and Agrawal, V. D. 1982. Statistical design verification. In Proceedings of the *Int. Fault Tolerant Computing Symposium*, 1982, 393-399.
- Hsiao, T.-C. and Seth, S. C. 1982. The use of Rademacher-Walsh spectrum in testing and design of digital circuits. In Proceedings of the *Int. Conference on Circuits and Computers (ICCC)*, 1982, 1-4.
- Agrawal, V. D., Seth, S. C. and Agrawal, P. 1981. LSI product quality and fault coverage. In Proceedings of the *18th Design Automation Conference*, 1981, 196-203.

Tam, S. C. and Seth, S. C. 1979. Portability of a high-level programming language for microcomputers: A case study. In Proceedings of the *9th Int. Symposium and Exhibition, Mini and Microcomputers*, 1979, 61-65.

Seth, S. C. and Kodandapani, K. L. 1975. Diagnosis of faults in linear tree networks. In Proceedings of the *13th Annual Allerton Conference*, 1975, 747-755.

Seth, S. C. 1973. Distance measures on fault detection test sets and their applications. In Proceedings of the *Int. Symposium on Fault Tolerant Computing*, 1973, 101-104.

Seth, S. C. 1969. Fault diagnosis of combinational cellular arrays. In Proceedings of the *7th Annual Allerton Conference*, 1969, 471-481.

## Chapters Authored

Padmanabhan, Raghav Krishna and Jandhyala, Ramana Chakradhar and Krishnamoorthy, Mukkai and Nagy, George and Seth, Sharad and Silversmith, William. 2009. Interactive Conversion of Web Tables. In *Graphics Recognition. Achievements, Challenges, and Evolution, (8th International Workshop, GREC 2009, La Rochelle, France, July 22-23, 2009. Selected Papers)*, LNCS #6020. Springer.

Jandhyala, Ramana C. and Krishnamoorthy, Mukkai and Nagy, George and Padmanabhan, Raghav and Seth, Sharad and Silversmith, William. 2009. From Tessellations to Table Interpretation. In *Intelligent Computer Mathematics, LNCS Vol. 5625*. Springer.

Bhattacharya, B. B. and Seth, S. and Zhang, S. 2009. Low-Energy Pattern Generator for Random Testing . In *Statistical Science and Interdisciplinary Research - Vol. 3: Algorithms, Architectures and Information Systems Security*. World Scientific, Singapore.

Seth, Sharad and Samal, Ashok. 2008. Feature Conflation (Invited Contribution) DOI: 10.1007/978-0-387-35973-1. In *Encyclopedia of GIS* . Springer.

Samal, Ashok and Seth, Sharad. 2008. Abstract Feature Extraction from Remotely Sensed Images of Urban Areas (Invited Contribution) DOI: 10.1007/978-0-387-35973-1. In *Encyclopedia of GIS, Part 9*. Springer.

Lopresti, Daniel and Nagy, George and Seth, Sharad and Zhang, Xiaoli. 2008. Multi-Character Field Recognition for Arabic and Chinese Handwriting. In *Lecture Notes in Computer Science, vol 4768*. Springer.

Scott, S. D. and Seth, S. and Samal, A. 1999. A Synthesizable VHDL Coding of a Genetic Algorithm. In *The Practical Handbook of Genetic Algorithms, Volume III: Complex Coding Systems*. CRC Press.

Nagy, G. and Samal, A. and Seth, S. and Fisher, T. and Guthmann, E. and Kalafala, K. and Li, L. and Sarkar, P. and Siovasubramaniam, S. and Xu, Y. 1998. A Prototype for Adaptive Association of Street Names with Streets on Maps. In *Lecture Notes in Computer Science, Vol: 1389K*. Springer.

Nagy, G. and Seth, S. and Viswanathan, M. 1997. DIA, OCR, and the WWW. In *Handbook of Optical Character Recognition and Document Image Analysis*. World Scientific.

Nagy, G. and Seth, S. 1996. Modern Optical Character Recognition. In *Encyclopedia of Telecommunications, Vol 11*. New York: Marcel Dekker.

Kenyon, P. and Seth, S. C. and Clematis, A. and Doderio, G. and Gianuzzi, V. 1992. Programming pipelined CAD applications on message passing architectures. In *Parallel Computing: From Theory to Sound Practice*. IOS Press.

Hudli, R. and Seth, S. C. 1989. Temporal logic based test generation for sequential circuits. In *CAD Systems Using AI Techniques*. North Holland.

Seth, S. C. and Agrawal, V. D. 1989. On the probability of fault occurrence. In *Defect and Fault Tolerance in VLSI Systems*. Plenum.

Agrawal, V. D. and Seth, S. C. 1988. Tutorial: Test Generation for VLSI Circuits. In *Tutorial: Test Generation for VLSI Circuits*. IEEE Computer Society Press.

Nagy, G. and Seth, S. C. and Stoddard, S. D. 1986. Document analysis with an expert system. In *Pattern Recognition in Practice II*. Elsevier Science.

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