Sharad C. Seth
(Curriculum Vitae)

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Education

B.E.(Hons.)	Electronics & Telecommunications	1964	Jabalpur, India
M.Tech	Electrical Engineering	1966	I.I.T. Kanpur, India
Ph.D.	Electrical Engineering	1970	U. of Illinois, Urbana-Champaign

Professional Experience

1983 – present, University of Nebraska-Lincoln, Professor, Computer Science & Engineering

Teaching, research and consulting. Led development of undergraduate degree program in Computer Engineering and the effort towards its successful accreditation by ABET; Supervised 10 PhDs, 19 Masters, and 34 undergraduate projects; Initiated courses and research in VLSI and Document Image Analysis; Grants over $1, 750, 000 as PI from NSF, NIMA, ARO, NATO, and AT&T Bell Labs; Offered short courses on VLSI Testing at leading international conferences, including International Test Conference, Design Automation Conference, European Test Conference, and International Conference on VLSI Design. Consulted with AT&T, GTE, NIH, GM-Delco, ABI (Omaha).

2005 – 2006, Sabbatical Leave

Research, consulting and short course: Lehigh University (one week) , Visiting Scientist at Intel, Santa Clara (8 weeks), Prabhu & Poonam Goel Chair in CSE at I. I. T. Kanpur (6 weeks), Visiting Scientist at Indian Statistical Institute, Kolkata (3 weeks), Visiting Faculty at Intel, Bangalore, India (3 weeks). Conducted research, initiated new collaborations with people at Intel on VLSI quality and reliability and at Lehigh on handwriting recognition; offered research seminars at Intel, Kanpur, Kolkata, and Bangalore.

1998 – 1999, Sabbatical Leave

Research, consulting and short courses. Visited University of California, Santa Barabra and initiated collaboration on a unified approach to design verification; Initiated work with researchers at the Indian Institute of Science, Bangalore, offered a short course on VLSI testing; Visited and gave a guest lecture at Texas Instruments, India.

1990 – 1991, Sabbatical Leave

Research and consulting. Worked at AT&T Bell Labs on multiprocessing for CAD applications and estimation of product quality of tested devices; Initiated collaboration with scientists at CNR, Italy and University of Genova under a NATO grant.

1996 – 2003, University of Nebraska-Lincoln, Director, Center for Communication and Information Science (CCIS), Interim during the first year

Research leadership. Led a group of thirty faculty associates from Computer Science & Engineering, Electrical Engineering, Engineering Mechanics, Mathematics, and Chemistry toward achieving the Center's goal of research excellence, research training of students, and Nebraska's economic development. During the full funding of this NRI Center, on a yearly basis, the associates multiplied internal funds more than three times with over thirty external grants. They collaborated with ten Nebraska businesses and government agencies; received many honors, awards, and patents and organized workshops and conferences in document image analysis, cryptography, combinatorics, and coding theory; and established the College of Arts & Sciences' Area of Excellence in Discrete and Experimental Mathematics. Organized lecture series on current topics such as electronic commerce, digital libraries, and quantum computing, bringing many prominent speakers to the campus.

1998 –2003, University of Nebraska-Lincoln, Coordinator, Research Computing Facility (RCF)

Research leadership. Initiated and led the effort towards NSF-EPSCoR funding to improve the infrastructure for high speed networking and for establishment of the Research Computing Facility (RCF), the first high-performance supercomputing facility available locally to the research scientists and engineers in Nebraska.

1976 – 1983, University of Nebraska-Lincoln, Associate Professor, Computer Science

Teaching, research and consulting. Developed integrated mini-micro laboratory under an NSF-LOCI grant; Initiated new courses in Microcomputer Applications, Logic Design Laboratory, VLSI Design, Computer Communications, and Computer Networks. Supervised 1 PhD, 6 Masters, and 35 undergraduate student projects. Initiated long-term research collaboration with scientists at AT&T Bell Laboratories.

1982 – 83, Sabbatical Leave, Visiting Associate Professor, I.I.T. Kanpur, India

Research and teaching. Supervised research and gave invited seminars at I.I.T. Madras and the Indian Institute of Science, Bangalore; Consultant, Semiconductor Complex, Chandigarh.

1970 – 1976, University of Nebraska-Lincoln, Assistant Professor, Computer Science

Teaching and research. Organized the first workshop on computer assisted instruction at UNL and developed the first course in Computer Science using self-paced instruction; Helped develop the joint CS 435/EE 477 (Switching Theory and Logic Design) course; Taught a variety of undergraduate and graduate courses, including computer architecture, discrete math, data structures, compiler theory, automata theory, formal languages, and computer communications; Supervised 5 Masters and 3 undergraduate projects.

1974 – 75, Sabbatical Leave, Visiting Assistant Professor, I.I.T. Kanpur, India

Research and teaching. Organized a UNESCO supported workshop on computer-assisted instruction at IIT Kanpur, India; Helped IITK initiate a PhD program in Computer Science.

Summer and Short-Term Appointments:

1980, 1982, and 1991: AT&T Bell Laboratories, Consultant, Member of Technical Staff

Worked in the 32-bit microprocessor design group analyzing tester data; Developed the n_0-model for a probabilistic analysis of tester data; Developed a new method of testing scan-based sequential circuits; Developed a model for analyzing performance of parallel VLSI CAD applications.

1986: Rensselaer Polytechnic Institute, Troy, New York

Worked at the Center for Integrated Electronics on problems in switch-level test generation. Initiated work on a joint proposal to US West on optical character recognition

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1992 and 1994: C. N. R. and University of Genova, Italy

Collaborated with researchers at the two institutions on a software pipeline model for parallelism under a NATO grant.

1993: NTH, Trondheim, Norway

Worked with E. Aas on design-error diagnosis using automated test generation techniques.

Professional Societies

IEEE (Fellow), ACM (Member), VLSI Society of India (Member)

RESEARCH

Major Research Accomplishments

Determining Product Quality from Test Data. The quality of a manufacturing test has traditionally been measured by fault coverage. However, there is no known direct relationship between the fault coverage of a test and the fraction of bad devices escaping detection by the test. My contribution is an analysis of test data that predicts the reject ratio. In 1980, while working with Drs. V. D. Agrawal and P. Agrawal at AT&T Bell Laboratories, I studied AT&T's microprocessor data and developed the now well-known n_0 model. This was further generalized in 1984. In 1985, at the invitation of Delco Electronics at Kokomo, Indiana, I studied their production data and observed that previous methods produced very pessimistic results. This led to the development of the latency model that takes into account the delayed detection of faults after their activation. This model has produced estimates of device quality with the closest agreement to actual data, when they are available. My recent work in this area was carried out in collaboration with IBM, Burlington, VT under support from NSF and at Intel, Santa Clara, as a Visiting Professor.

A Theory of Testability. V. D. Agrawal of Bell Laboratories and I described the testing behavior of an entire circuit, irrespective of its size, by a single function called the detection probability distribution. As the exact computation of this distribution has exponential complexity, we devised a supergate partitioning method that allows exact computation in many cases and close approximations in others. The supergate analysis framework, originally intended to simplify problems in test generation and design for testability, has since also been used by others in power analysis.

XY-Trees. While optical character recognition has a long history, its encompassing discipline of document image analysis (DIA) came into its own only in the 1980's when the costs of scanning, computing, and storage could be afforded by consumers. During the infancy of DIA, G. Nagy and I proposed the XY-tree data structure for page segmentation that has since been widely used in page layout analysis of technical documents by us and others. Recently, the data structure has been the basis of a highly accurate adaptive algorithm for page segmentation and analysis of web-table headers for extraction of semantic structure.

Map Image Understanding. Worked with G. Nagy, A. Samal, and six students (one PhD, three Masters, and two undergraduates) on automated techniques to convert a large volume of topographic maps. The specific problem studied was the extraction and recognition of street lines and labels from the scanned image of a map and to produce a database of association between street segments and labels. The project was funded by the National Imagery and Mapping Agency (NIMA) to advance the state of the art in map image analysis. The unique aspect of this work was its emphasis on adaptation during the conversion of a batch of maps.

Honors and Awards

IEEE Fellow Award "For contributions to testing of digital electronics circuits", 1997.

Best Poster Paper Award, *3rd International Conference on Document Analysis and Recognition*, 1995.

Honorable Mention Paper Award, *International Conference on VLSI Design*, 1992.

Best Paper Award, Design and Test Category, *International Conference on Computer Design*, 1988.

Best Presentation Paper Award, *International Conference on Computer Design*, 1985.

Grants

(PI) Coverage Metrics for Test Sequences, $40, 000, Intel Corporation. 2007-2008.

(PI) High Level Coverage Metrics for HVM & Validation, $60, 647, 2005-2007.

(PI) Coverage Metrrics for Validation Tests, $30, 000, 2004-2005.

(CoPI) High Level Interpretation and Feature Extraction of Satellite Imagery And Historical Aerial Photography, (PI A. Samal), NASA Nebraska Space Grant & EPSCoR, $12, 000, 2004-2005.

(CoPI) Acquisition of High Performance Computing and Data Visualization for Scientists and Engineers, (PI R. Sincovec), $500, 000, NSF, 2003-2006.

(CoPI) MRI: Acquisition of High Performance Computing and Data Visualization for Scientists and Engineers, (PI R. Sincovec), $600, 000, NSF, 2003-2006.

(CoPI) UNL Priority Area Proposal in Simulation, Computing Engineering, and Information Technology (PI: R. Sincovec), $600, 000, 2002-2004.

(PI) NSF International Program. "US-India Cooperative Research: A new approach to Boolean division that can trade performance for computation", (coPI: Prof. S. Biswas at I.I.T. Kanpur), $10, 000, 3/1/02 – 2/28/05.

(PI) NSF, "A Unified Approach to Testing and Verification of Designs Synthesized from High-Level Specifications," $390, 561 (plus CCIS match), (CoPIs: K-T. Cheng – UCSB, S. K. Mehta, and K. Einspahr), 9/1/1999 – 2/28/2003.

(PI) NSF, REU Supplement to the above grant, $5, 000, granted 2/12/03.

(CoPI) NU NRI, "Geospatial Data Integration for Decision Support," (PI: S. Reichenbach,), over $200, 000/year, UNL, 1998-2003.

(PI) NSF, "An Analysis of Sematech Test Data to Predict Reject Ratio," $115, 541 (plus $20, 300 CCIS match), 7/1/98 – 12/31/2001 (CoPI: S. Mehta).

(PI) NSF EPSCoR, "Nebraska EPSCoR Cooperative Agreement," $711, 715 (plus $768, 852 match), 1/1/98 – 8/31/2001 (RCF Grant).

(PI) National Imagery and Mapping Agency (NIMA), "Reading Street Names from Maps," $124, 894 and $24, 324 match from UNL-CCIS; (CoPIs: G. Nagy (RPI) and A. Samal), 0/1/96 – 12/31/97.

(PI) Nebraska Department of Roads, "Video Traffic Accident Investigation," $116, 555 and $56, 622 match from Omaha Police Department, UNL-CCIS, and UNL-CIR; (CoPIs: S. Reichenbach, P. McCoy, and A. Samal); 9/19/96 – 1/6/98.

(CoPI) DEPSCoR, ARO, "Prototype for an Open Intelligent Information System," $266, 040 and $137, 019 match from UNL-CCIS; (PI: J. Deogun), 6/1/96 – 5/31/99 (Co-PI).

(PI) American Business Information, Omaha, "Decoding Images of Formatted Reference Documents," $25, 469 and $5094 match from UNL-CCIS; (CoPI: A. Samal), 10/4/95 – 5/31/97.

(PI) NATO, Brussels, Belgium: "Programming Environment and CAD Software Development for Parallel Computers," $10, 610 (Collaborative Research Grant with A. Clematis of C. N. R. Genova, Italy); 12/15/90 – 3/31/94.

(PI) NSF: "Design for Testability and Test Generation with Multiple Clocks," $67, 953 (includes ROA and REU supplements), 3/15/91 – 6/28/93.

(PI) AT&T Bell Labs, Murray Hill, NJ: "A High Level Program Development Environment for MARS," $107, 898 and $47, 438 match from UNL-CCIS; 9/21/89 – 6/30/93.

(Co-PI) US West: "Digitized Document Analysis," Phases I and II $230, 000; with G. Nagy (RPI); 8/3//87 – 8/2/89.

(PI) NSF: "Decoding substitution ciphers with OCR applications," $53, 885; (CoPI: G. Nagy, RPI), 6/15/85 – 5/31/87.

(CoPI) NSF: "Laboratory for research on two-dimensional problems," $82, 900; with R. Keller; 1984.

(PI) NSF: "Integrated Mini-microcomputer Learning Center," $13, 100; (CoPI: G. Nagy), 4/15/77 – 8/31/79.

(CoPI) NSF: "Register-transfer modules," $12, 600; (PI: A. Lambert), 1973.

Donations and Gifts

(PI) Donation of 8 HP laptops for use in outreach activity by CSE Department, $8, 000, 2007.

(PI) Xilinx, Inc., Donation of CAD tools and evaluation board for FPGA-based designs, commercial price $44, 289, university price $4879; 12/4/97.

(PI) ACM: "SIGDA: DALibrary," Award of an electronic library on 8 CD-ROM's containing page images and text of design automation literature for the past twenty five years, 1992 (donated to UNL Libraries).

(PI) Cadence, Massachusetts (Educational Gift), Production quality software for circuit description and simulation (Verilog), fault simulation (Verifault), and test generation (Testscan) to be used for research and instruction, 1992.

(PI) Mentor Graphics (Educational Gift), Donation of a complete set of production quality software tools for design of VLSI chips and circuit boards, 1989 and 1992.

(PI) Hewlett Packard: (Equipment Grant) Scanner and Paintjet printer, 1987.

1. REFEREED PUBLICATIONS

(In reverse chronological order).

Journals

1. Z. Chen, S. Seth, D. Xiong, and B. B. Bhattacharya, “PVT: Unified Reduction of Test Power, Volume, and Test Time using Double-Tree Scan Architecture”, (Under review)

2. G. Nagy, S. Seth, and M. Viswanathan, "Project methods require black border removal", accepted *IEEE Transactions on Pattern Analysis and Machine Intelligence (PAMI),* April 2009, p. 762.
3. I. Saha, B. B. Bhattacharya, S. Zhang, and S. C. Seth, "Planar straight-line embedding of double-tree scan architecture on a rectangular grid" *Fundamenta Informaticae*, 89.2 (2008): 331-344.
4. Samal, S. C. Seth, and K. Cueto, "A Feature-Based Approach to Conflation of Geospatial Sources", *Int. Journal of Geographic Information Science,* 18.5: 459-489, 2004.

5. H. Cui, S. C. Seth, and Shashak K. Mehta, "Modeling Fault Coverage of Random Test Patterns", *Journal of Electronic Testing: Theory & Applications (JETTA),* 19(3):271-284, 2003.

6. L. Li, G. Nagy, A. Samal, S. Seth, Y. Xu, "Integrated Text and Line Extraction from a Topographic Map", *Int Jour. Document Analysis and Recognition (IJDAR), Springer,* 2(4):177-185, 2000.

7. K. Einspahr, S. K. Mehta, and S. C. Seth, "A Synthesis for Testability Scheme for Finite State Machine UsingClock Control", *IEEE Trans Computer Aided Design,* 18(12):1780-1792, 1999.

8. Y. Yu, A. Samal, and S. Seth, "A system for Recognizing a Large Class of Engineering Drawing", *IEEE Transactions on Pattern Analysis and Machine Intelligence,* 19((8)):868-890, 1997.

9. K. Einspahr and S. C. Seth, "A Switch-Level Test Generation System for Synchronous and AsynchronousCircuits", *Journal of Electronic Testing: Theory and Applications (JETTA),* 6(1):59-73, 1995.

10. P. Kenyon, S. Seth, P. Agrawal, A. Clematis, G. Dodero, and V.Gianuzzi, "Programming Pipelined CAD Applications on Message PassingArchitectures", *Concurrency Practice and Experience,* 7(4):315-337, 1995.

11. Y. Yu, A. Samal and S. Seth, "Isolating Symbols from Connection Lines in a Class of Engineering Drawings.", *Pattern Recognition,* 27(3):391-404, 1994.

12. D. V. Das, S. Seth, and V. D. Agrawal, "Accurate Computation of Field Reject Ratio Based on Fault Latency", *IEEE Trans. on VLSI Systems,* 1(4):537-545, 1993.

13. M. Krishnamoorthy, G. Nagy, S. Seth, and M. Viswanathan, "Syntactic segmentation and labeling of digitized pages from technical journals", *IEEE Transaction on Pattern Analysis and Machine Intelligence,* 15(7):737-747, 1993.

14. M. Krishnamoorthy, P. Molholt, G. Nagy, S. Seth, and M. Viswanathan, "Tools for Document Image Utility", *Library Hi Tech,* 11(3):73-92, 1993.

15. P. Agrawal, V. D. Agrawal, and S. C. Seth, "A new method for generating tests for delay faults in non-scan circuits", *IEEE Design & Test of Computers,* 10(1):20-28, 1993.

16. G. Nagy, S. Seth, and M. Viswanathan, "A prototype document image analysis system for technical journals", *IEEE Computer,* 25(7):10-22, 1992.

17. S. C. Seth, V. D. Agrawal, and H. Farhat, "A statistical theory of digital circuit testability", *IEEE Trans. Computers,* 38(11):582-586, 1990.

18. B. B. Bhattacharya and S. C. Seth, "Design of parity testable combinational circuits", *IEEE Transactions on Computers,* 38(11):1580-1584, 1989.

19. L. L. Lipsky and S. C. Seth, "Signal probabilities in And-Or trees", *IEEE Transactions on Computers,* 38(11):1558-1563, 1989.

20. S. C. Seth and V. D. Agrawal, "A new model for computation of probabilistic testability in combinational circuits", *Integration, the VLSI Journal,* 7(1):49-75, 1989.

21. G. Nagy, S. Seth, and K. Einspahr, "Decoding substitution ciphers by means of word matching with application to OCR", *IEEE Trans. Pattern Analysis and Machine Intelligence,* 9(5):710-715, 1987.

22. S. C. Seth and V. D. Agrawal, "A review of testing of digital devices. Invited review", *IETE Technical Review, The Institute of Electronics and Telecommunications Engineers, India,* 2(11):363-374, 1985.

23. S. C. Seth and V. D. Agrawal, "Cutting Chip Testing Costs", *IEEE Spectrum,* 22(4):38-45, 1985.

24. S. C. Seth and V. D. Agrawal, "Characterizing the LSI yield equation from chip test data", *IEEE Trans. Computer-Aided Design,* 3(4):123-126, 1984.

25. T.-C. Hsiao and S. C. Seth, "The use of Rademacher-Walsh spectrum in random compact testing", *IEEE Transactions on Computers,* 33(10):934-937, 1984.

26. S. C. Seth and L. L. Lipsky, "A simplified method to calculate failure times in fault-tolerant systems", *IEEE Transactions on Computer,* 32(8):754-756, 1983.

27. V. D. Agrawal, S. C. Seth, and P. Agrawal, "Fault coverage requirements in production testing of LSI circuits", *IEEE Solid State Circuit Journal,* SC-17:57-61, 1982.

28. S. C. Seth and K. Narayanaswamy, "A graph model for pattern-sensitive faults in random access memories", *IEEE Trans. on Computers,* 30(12):973-977, 1981.

29. S. C. Seth and V. D. Agrawal, "Forecasting field-reject rate of LSI chips", *IEEE Electronic Device Letters,* EDL-2(11):286-287, 1981.

30. K. L. Kodandapani and S. C. Seth, "On combinational networks with restricted fanout", *IEEE Trans. on Computers,* 27(4):309-318, 1978.

31. J. M. Steckelberg and S. C. Seth, "On a relation between algebraic programs and Turing machines", *Information Processing Letters,* 6:180-183, 1977.

32. S. C. Seth, "Data compression techniques in logic testing: An extension of transition counts", *Journal of Design Automation and Fault Tolerant Computing,* 1(2):90-114, 1977.

33. S. C. Seth and K. L. Kodandapani, "Diagnosis of faults in linear tree networks", *IEEE Trans. on Computers,* 26(1):29-33, 1977.

Book

V. D. Agrawal and S. C. Seth,"Tutorial: Test Generation for VLSI Circuits", *Tutorial: Test Generation for VLSI Circuits,*IEEE Computer Society Press, 1988.

Book Chapters

1. R. Padmanabhan, R. C. Jandhyala, M. Krishnamoorthy, G. Nagy, S. Seth, W. Silversmith, "Interactive Conversion of Web Tables" Lecture Notes in Computer Science (LNCS), Ed.Jean-Marc Ogier, Liu, Wenyin, and Josep Llados. Springer, 2010.

2. B. B. Bhattacharya, S. C. Seth, and S. Zhang. "Low-energy pattern generator for random testing," i *Algorithms, Architectures, and Information Systems Security*, (Statistical Science and Interdisciplinary Research, vol. 3), World Scientific, Singapore, Chapter 8, pp. 117-138, 2009.

3. D. Lopresti, G. Nagy, S. Seth, and X. Zhang."Multi-Character Field Recognition for Arabic and Chinese Handwriting" *Lecture Notes in Computer Science*, Ed.D. Doermann and S. Jaeger, Springer, Vol. 4768, pp. 218-230, March 2008.

4. S. Seth and A. Samal."Feature Conflation", Invited Contribution, *Encyclopedia of GIS*, Ed.H. Xiong and S. Shekhar, pp. pp. 129-133, Springer, 2008.

5. A. Samal and S. Seth."Abstract Feature Extraction from Remotely Sensed Images of Urban Areas", Invited Contribution, *Encyclopedia of GIS*, Ed.H. Xiong and S. Shekhar, pp. pp. 314-320, Springer, 2008.

6. S. Zhang, S. Seth, and B. B. Bhattacharya."Low-power BIST design" *ISI Platinum Jubilee Commemorative Volume*.Ed.B. B. Bhattacharya, C. A. Murthy, B. B. Chaudhuri, and B. Chanda. Singapore: World Scientific, 2008.

7. S.D. Scott, S. Seth and A. Samal,"A Synthesizable VHDL Coding of a Genetic Algorithm", *The Practical Handbook of Genetic Algorithms, Volume III: Complex Coding Systems,*Ed: Lance A. Chambers,pp. 239-268,CRC Press, 1999.

8. G. Nagy, A. Samal, S. Seth, T. Fisher, E. Guthmann, K. Kalafala, L. Li, P. Sarkar, S. Siovasubramaniam, and Y. Xu,"A Prototype for Adaptive Association of Street Names

with Streets on Maps", *Lecture Notes in Computer Science, Vol: 1389K,*Ed: C. Tombre and A. Chhabra ,pp. 302-313,Springer, 1998.

9. G. Nagy, S. Seth, and M. Viswanathan,"DIA, OCR, and the WWW", *Handbook of Optical Character Recognition and Document Image Analysis,*Ed: H. Bunke and P.S.P. Wang,pp. 729-750,World Scientific, 1997.

10. Nagy, G. and S. Seth,"Modern Optical Character Recognition", *Encyclopedia of Telecommunications, Vol 11,*Ed: F.E. Froehlich and A. Kent,pp. 473-531,New York: Marcel Dekker, 1996.

11. P. Kenyon, S. C. Seth, A. Clematis, G. Dodero, and V. Gianuzzi,"Programming pipelined CAD applications on message passing architectures", *Parallel Computing: From Theory to Sound Practice,*pp. 550-553,IOS Press, 1992.

12. R. Hudli and S. C. Seth,"Temporal logic based test generation for sequential circuits", *CAD Systems Using AI Techniques,*Ed: I. G. Odawara,pp. 85-92,North Holland, 1989.

13. S. C. Seth and V. D. Agrawal,"On the probability of fault occurrence", *Defect and Fault Tolerance in VLSI Systems,*Ed: I. Koren,pp. 47-52,Plenum, 1989.

14. G. Nagy, S. C. Seth, S. D. Stoddard,"Document analysis with an expert system", *Pattern Recognition in Practice II,*Ed: E. S. Gelsema and L. N. Kanal,pp. 149-159,Elsevier Science, 1986.

Conferences

1. D. Zhan, H. Jiang, S. Seth, “STEM: Spatiotemporal Management of Capacity for Intra-Core Last Level Caches”, (Under review).

2. N. Schemm, S. Balkir, and S. Seth. “Hardware Implementation of the Double-Tree Scan Architecture”, *Int. Symposium on Circuits and Systems* (ISCAS), 2010, to be published.

3. S. Seth, R. Jandhyala, M. Krishnamoorthy, and G. Nagy. “Analysis and Taxonomy of Column Header Categories for Web Tables”, *Proc. 9th IAPR Workshop on Document Analysis and Systems* (DAS), 2010), pp. 81-88.

4. Z. Chen, S. Seth, D. Xiang. “A Novel Hybrid Delay Testing Scheme with Low Test Power, Volume, and Time” *Proc. VLSI Test Symposium* (VTS), DOI 10.1109/VTS.2010.5469547, 2010, pp. 307-312.

5. D. Zhan, H. Jiang, S. C. Seth. "Exploiting Set-Level Non-Uniformity of Capacity Demand to Enhance CMP Cooperative Caching." *Proc. International Parallel & Distributed Processing Symposium (IPDPS)*, DOI 10.1109/IPDPS.2010.5470441, pp. 1-10, 2010.

6. S. Seth, Z. Chen, D. Xiang, and B. B. Bhattacharya. “A Unified Solution to Scan Test Volume, Time, and Power Minimization”, *Proc. International Conference on VLSI Design,* pp. 9-14, 2010.

7. R. Padmanabhan, R. C. Jandhyala, M. Krishnamoorthy, G. Nagy, W. Silversmith, S. Seth. "How many different kinds of tables are there?." proc. *8th IAPR Workshop on*

Graphics Recognition (GREC) at: http://www.univ-lr.fr/colloque/grec2009/proceedings_avecCouverture.pdf, pp. 32-43, 2009, .

8. G. Nagy, S. Seth, W. Silversmith, M. Krishnamoorthy, R. C. Jandhyala, and R. Padmanabhan. "From isothetic tessellations to web tables." 8th International Conference *Mathematical Knowledge Management* (MKM 2009), published in *Intelligent Computer Mathematics,* Lecture Notes in Computer Science, vol. 5625, pp. 422-437, Springer, 2009.

9. J. Kang, S. Seth, Y-S. Chang, V. Gangaram. "Efficient Selection of Observation Points for Functional Tests", *9th International Proc. Symposium on Quality Electronic Design (ISQED),* pp. 236-241, 2008.

10. J. Kang, S. C. Seth, and S. K. Mehta. "Symbolic Path Sensitization Analysis and Applications", *16th Asian Test Symposium (ATS)*, pp. 439-444, 2007.

11. J. Kang, S. C. Seth, and V. Gangaram. "Efficient RTL Coverage Metric for Functional Test Selection", *25th IEEE VLSI Test Symposium (VTS),* pp. 318-324, 2007.

12. D. Lopresti, G. Nagy, S. Seth, and X. Zhang. "Multi-Character Field Recognition for Arabic and Chinese Handwriting." *Summit on Arabic and Chinese Handwriting (SACH),* pp. 93-100, 2006.

13. A. Joshi, G. Nagy, Dan Lopresti, S. C. Seth. "A Maximum-Likelihood Approach to Symbolic Indirect Correlation", *International Conference on Pattern Recognition (ICPR)*, pp. 99-103, 2006.

14. S. Zhang, S. C. Seth, and B. B. Bhattacharya. "Efficient test compaction for pseudo-random testing", *Asian Test Symposium (ATS),* pp. 337-342, 2005.

15. S. Zhang, S. C. Seth, and B. B. Bhattacharya. "On Finding Consecutive Test Vectors in a Random Sequence for Energy-Aware BIST Design", *Proc. 18th Int. Conf. on VLSI Design*, pp. 491-496, 2005.

16. L. Lin, A. Samal, and S. Seth. "Context Directed Interpretation of Remotely Sensed Urban Images." *ASPRS 2004 Fall Conference*, pp. 1-9, 2004.

17. G. Nagy, D. Lopresti, M. Krishnamoorthy, Y. Lin, S. Mehta, and S. Seth,"A Nonparametric Classifier for Unsegmented Text", *Document Recognition and Retieval XI (part of IS&T/SPIE Int. Symposium on Electronic Imaging 2004),* IS&T/SPIE, 6 pp., January 2004

18. B. B. Bhattacharya, S. C. Seth, and S. Zhang,"Double-Tree Scan: A Novel Low-Power Scan-Path Architecture", *International Test Conference (ITC),* IEEE Computer Society, pp. 470-479, October 2003.

19. B. B. Bhattacharya, S. C. Seth, and S. Zhang,"Low-Energy BIST Design for Scan-Based Logic Circuits", *16th Int Conference on VLSI Design,* VSI, IEEE CS, ACM SIGDA, 546-551, January 2003

20. G. Nagy, S. C. Seth, S. K. Mehta, and Y. Lin,"Indirect Symbolic Correlation Approach to Unsegmented Text Recognition", *DIAR: Workshop on Document*

Image Analysis and Retrieval (in conjunction with CVPR'03), available through IEEE Digital Library, IAPR, 8 pp., June 2003.

21. H. Cui and S. Seth,"A Novel method to improve the test efficiency of VLSI tests", *15th International Conference on VLSI Design (ASP-DAC/VLSI Design 2002),* VSI, IEEE CS, ACM SIGDA, 499-504, January 2002.

22. G. Nagy and S. Seth,"Twenty questions for document classification", *Document Layout Interpretation and its Applications Workshop,* , Invited lead presentation to the workshop.

23. M. W. Weiss, S. C. Seth, S. K. Mehta, and K. L. Einspahr,"Design Verification and Functional Testing of Finite State Machines", *International Conference on VLSI Design – VLSI Design 2001,* VLSI Society of India, IEEE Comp Society, & ACM SIGDA, 189-195, January 2001.

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32. P. T. McCoy, S. C. Seth, S. E. Reichenbach, and A. Samal,""Digital Camera Traffic Accident Investigation System"", *1998 Transportation Conference Proceedings, Crossroads 2000,* 159-163, August 1998.

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36. G. Nagy, A. Samal, S. Seth, T. Fisher, E. Guthmann, K. Kalafala, L. Li, S. Sivasubramaniam, and Y. Xu,""Reading Street Names from Maps -- Technical Challenge"", *Proceedings GIS/LIS Conference,* 89-97, October 1997.

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40. S. D. Scott, A. Samal, and S. Seth,"HGA: A Hardware-Based Genetic Algorithm", *Symposium of Field Programmable Gate Arrays,* ACM/SIGDA, 53-59, 1995.

41. S. Venkataraman, S. Seth, and P. Agrawal,"Parallel Test Generation with Low Communication Overhead", *8th Int Conf VLSI Design,* VLSI Society of India, ACM/SIGDA, 116-120, January 1995.

42. D. Sylwester and S. Seth,"A Trainable, Single-Pass Algorithm for Column Segmentation", *Third Int Conf Document Analysis and Recognition (ICDAR),* IAPR et al., 615-618, August 1995.

43. Y. Yu, A. Samal, and S. C. Seth,"A System for Recognizing a Large Class of Engineering Drawings", *Third Int Conf Document Analysis and Recognition (ICDAR),* IAPR et al., 791-794, August 1995.

44. S. Seth, L. Gowen, M. Payne, and D. Sylwester,"Logic Simulation using an Asynchronous Parallel Discrete- Event Simulation Model on SIMD Machine", *Proc. 7th Int. Conference on VLSI Design,* VSI, IEEE-CAS, ACM-SIGDA, 29-32, 1994.

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46. K. L. Einspahr, S. C. Seth, and V. D. Agrawal,"Clock Partitioning for Testability", *Proc. Third IEEE Great Lakes Symposium on VLSI (GLSVLSI),* 42-46, March 1993.

47. K. Einspahr and S. C. Seth,"A switch-level test generation system", *Proc. Int. Conference on VLSI Design,* VSI, IEEE-CAS, ACM-SIGDA, 43-48, January 1992.

48. P. Agrawal, V. D. Agrawal, and S. C. Seth,"Dynamic timing analysis with partial scan activation in sequential circuits", *Proc. Euro-DAC/Euro-VHDL 92,* 138-141, September 1992.

49. D. V. Das, S. C. Seth, V. D. Agrawal,"Estimating the quality of manufactured digital sequential circuits", *Proc. Int. Test Conference (ITC),* 210-217, 1991.

50. V. D. Agrawal, S. C. Seth, and J. S. Deogun,"Design for testability and test generation with two clocks", *Proc. Int. Conference on VLSI Design,* VSI, IEEE-CAS, ACM-SIGDA, 112-117, January 1991.

51. V. Sivaramakrishnan, S. C. Seth, and P. Agrawal,"Parallel test pattern generation using boolean satisfiability", *Proc. Int. Conference on VLSI Design,* VSI, IEEE-CAS, ACM-SIGDA, 69-74, January 1991.

52. D. V. Das, S. C. Seth, P. T. Wagner, J. C. Anderson, and V. D. Agrawal,"An experimental study on reject ratio prediction for VLSI circuits: Kokomo revisited", *Proc. Int. Test Conference (ITC),* IEEE, 712-720, 1990.

53. P. Kenyon, P. Agrawal, and S. Seth,"High-level microprogramming: An optimizing compiler for a processing element of a CAD accelerator", *Proc. 23rd Int.Symp. and Workshop on Microprogramming and Microarchitectur,* 97-106, 1990.

54. R. Hudli and S. C. Seth,"Testability analysis of synchronous sequential circuits based on structural data", *Proc. Int. Test Conference (ITC),* IEEE, 364-372, 1989.

55. S. C. Seth, V. D. Agrawal, and H. Farhat,"A theory of testability with applications to fault coverage analysis", *Proc. 1st European Test Conference (ETC),* 139-143, 1989.

56. V. D. Agrawal, H. Farhat, and S. C. Seth,"Test generation by fault sampling", *Proc. Int. Conference on Computer Design (ICCD),* 58-61, 1988.

57. W. Ke, S. C. Seth, and B. B. Bhattacharya,"A fast fault simulation algorithm for combinational circuits", *Proc. Int. Conference on Computer Aided Design (ICCAD),* 166-169, 1988.

58. R. Hudli, W. Ke, and S. C. Seth,"Structural profile of benchmark circuits relating to the test generation problem", *Proc. Second Int. Conference on VLSI Design,* VSI, IEEE-CAS, ACM-SIGDA, 438-447, January 1988.

59. S. C. Seth,"What is the path to fast fault simulation? Invited panelist statement", *Proc. Int. Test Conference (ITC),* 186-188, September 1988.

60. B. B. Bhattacharya and S. C. Seth,"On the reconvergent structure of combinational circuits with applications to compact testing", *Proc. 17th Int. Symposium. on Fault Tolerant Computing (FTCS),* 264-269, 1987.

61. G. Nagy, S. Seth, K. Einspahr, and T. Meyer,"Efficient algorithms to decode substitution ciphers with applications to OCR", *Proc. 8-th Int. Conference on Pattern Recognition (ICPR),* 352-355, 1986.

62. S. C. Seth, B. B. Bhattacharya, and V. D. Agrawal,"An exact analysis for efficient computation of random- pattern testability in combinational circuits", *Proc. 16th Int. Symposium on Fault Tolerant Computing (FTCS),* 318-323, 1986.

63. S. C. Seth,"Predicting fault coverage from probabilistic testability. Invited contribution as a panelist", *Proc. Int. Test Conference (ITC),* 803-805, 1985.

64. S. C. Seth and R. Muralidhar,"Analysis and design of robust data structures", *Proc Int.Fault Tolerant Computing Symposium (FTCS),* 14-19, 1985.

65. S. C. Seth, L. Pan, and V. D. Agrawal,"PREDICT - Probabilistic Estimation of Digital Circuit Testability", *Proc Int.Fault Tolerant Computing Symposium (FTCS),* 220-225, 1985.

66. V. D. Agrawal and S. C. Seth,"Probabilistic testability", *Proc. Int. Conference on Computer Design (ICCD),* 562-565, 1985.

67. V. D. Agrawal, S. C. Seth, C. C. Chuang,"Probabilistically guided test generation", *Proc. Int. Symposium on Circuits and Systems (ISCAS), .* 687-690, 1985.

68. G. Nagy and S. C. Seth,"Hierarchical image representation with application to optically scanned documents", *Proc. 7th Int. Conference on Pattern Recognition (ICPR),* 347-349, 1984.

69. S. C. Seth and V. D. Agrawal,"Statistical design verification", *Proc. Int. Fault Tolerant Computing Symposium (FTCS),* 393-399, 1982.

70. T.-C. Hsiao and S. C. Seth,"The use of Rademacher-Walsh spectrum in testing and design of digital circuits", *Proc. Int. Conference on Circuits and Computers (ICCC),* 1-4, 1982.

71. V. D. Agrawal, S. C. Seth, and P. Agrawal,"LSI product quality and fault coverage", *Proc. 18th Design Automation Conference (DAC),* ACM/IEEE, 196-203, 1981.

72. S. C. Tam and S. C. Seth,"Portability of a high-level programming language for microcomputers: A case study", *Proc. 9th Int. Symposium and Exhibition, Mini and Microcomputers,* 61-65, 1979.

73. S. C. Seth and K. L. Kodandapani,"Diagnosis of faults in linear tree networks", *Proc. 13th Annual Allerton Conference,* 747-755, 1975.

74. S. C. Seth,"Distance measures on fault detection test sets and their applications", *Proc. Int. Symposium on Fault Tolerant Computing (FTCS),* IEEE Computer Society, 101-104, 1973.

75. S. C. Seth,"Fault diagnosis of combinational cellular arrays", *Proc. 7th Annual Allerton Conference,* 471-481, 1969.

TEACHING AND OUTREACH

Course Taught

Sophomore: Computer Organization, Discrete Mathematics

Junior: Fortran for Social Scientists, Logic Design, Data Structures

Senior/Graduate: Computer Architecture, Computer Communications, Language Structures, Microcomputer Applications, Computer Communications, Computer Networks, VLSI Design, Operating Systems, Professional Development, Senior Design, Geographic Information Analysis

Graduate: Automata Theory, Formal Languages, VLSI Testing

Graduate Seminars: Fault Tolerant Computing, VLSI Theory & Design, Computer Networks, Design Automation, Parallel CAD Algorithms, High-Level Synthesis

Educational Programs Developed/Delivered

Organizer and Speaker: Tutorial on "Test Generation for VLSI Circuits", International Test Conference (1987, 88, 89, 90), Design Automation Conference (1989), First European Test Conference (1989), VLSI Design Conference (1992 and 95).

Short Course on VLSI Testing at Indian Institute of Science Bangalore, India, 1999 to over 40 participants from the industry and the Institute.

New and Innovative Teaching Activities

Prepared and taught a new senior/graduate level seminar course on *Geographic Information Analysis*.

Prepared and taught a new graduate seminar course on *High-Level Synthesis of Digital Systems* (1995).

Prepared and taught a new graduate seminar course on *Parallel Algorithms for Computer Aided Design* (1992).

Prepared and taught a new graduate seminar course on *Design Automation Algorithms* (1987, and 89).

Prepared and taught a new course on *VLSI Design*, first as a graduate seminar (1981 and 1984) and later as a senior/graduate seminar course (1986). In 1987 this became a regular senior/graduate course (CS 434/834).

Prepared and taught a new senior/graduate course on *Computer Networks* at IIT Kanpur, India, and UNL (1983).

Developed CS 336, a new 1-hr junior-level lab course on *Logic Design* (1981).

Prepared and taught a new graduate seminar course on *Testing of Very Large Scale Integrated (VLSI) Circuits* (1978); it later became a regular graduate-level course (CSCE 932).

Introduced microcomputers for the first time at UNL through a grant from NSF; supervised several student projects on microcomputers, developed a new senior/graduate course and associated laboratory on *Microcomputer Applications* (1976-77).

Prepared and taught a senior/graduate *Computer Communications* course for the first time at UNL (1976).

Organized workshops on *Computer Assisted Instruction* (CAI) at UNL and Indian Institute of Technology, Kanpur (1974); introduced the PLATO system at UNL.

Prepared unit notes and tests for a self-paced *Discrete Structures* course, taught under the Keller Plan (1973).

Direction of Graduate Student Research as Major Advisor

11 PhD and 25 Masters students have graduated under my supervision. Five PhD students work in Nebraska - three are professors (Kent Einspahr and Don Sylwester at Concordia University and Hassan Farhat at UNO), the other two (Paul Kenyon and Bill Mahoney) have very successful startup businesses of their own. Among the rest, Yuhong Yu works at Lucent Bell Laboratories at Holmdel, NJ; V. Sivaramakrishnan and Dharmavir Das work for companies in Silicon Valley; Raghu Hudli worked for IBM Research in the US before starting his own company in India in object-oriented technology. Ten-Chuan Hsiao taught in California and worked for Kennedy, a magnetic storage device company. Hailong Cui works for Qualcomm, Sheng Zhang is employed at Broadcom, and Jian Kang works at Intel. All my Master's students have very successful careers and most of them have challenging jobs in Silicon Valley.

Significant Outcome of Educational Programs

Chaired the joint CS/EE Committee to design a new undergraduate curriculum in Computer Engineering (1987-90), supervised its introduction in 1991 and led the effort towards its successful ABET accreditation in 1996. This program now has an enrollment of more than 300 students.

SERVICE

University Service

(Major committee assignments since 1985)

- Supervision of JDE Design Studio Project on Graduate Admissions and Management System (GAMES), July 2007-August 2008.
- College of Engineering Equity Committee(CET) 2003 –
- J. D. Edwards Honors Program – Executive Director Search (UNL): 2000-01
- Faculty Search Committee Chair (CSE Department): 2000-01.
- Joint CSE/EE Comp Eng Curriculum Committee (Coordinator): 1996-present
- CSE Chair Search (CAS): 1999-2000
- EE Chair Search (CET): 1999-2000
- Computational Services and Facilities Committee (UNL): 1995-98)
- Faculty Search Committee Chair (CSE Department): 1997-98.
- Advisory Committee, Int. Student Affairs (UNL): 1995-98
- Promotion and Tenure Committee (CET): 1993-94, 1996-97
- Faculty Advisory Committee to Omaha Institute (UNL): 1996-97
- Chair, Committee to write ABET report for accreditation of B.S. (Comp Eng) program (CSE Department): 1996
- Academic Program Council (UNL): 1994-95
- Academic Senate (UNL): 1992-95
- Faculty Research Advisory Committee (CET): 1990-94
- Chair, Joint CSE/EE Committee to develop undergraduate Computer Engineering program (CET): 1987-90

Professional Service

- Member of Editorial Board, Journal of Electronic Testing: Theory and Applications (JETTA), 1990 – present.
- Associate Editor (Testing Area), IEEE Transactions on Computer Aided Design, 1989-1992.
- Editor (Tutorials and Short Papers), IEEE Design & Test of Computers, 1987-1991.
- Program Committee Chair, EIT 2005.
- Program Committee Member, IEEE VLSI Design Conference, 1989 - present.
- Program Committee Member, Asian Test Symposium, 1994, 1995, 2000, and 2001.
- Invited Panelist, *International Test Conference* (1985, 88, and 90) and *International Symposium on Circuits and Systems*, 1985.
- Program Committee Member, 19th International Symposium on Fault tolerant Computing, 1989.
- Program Committee Member, Third Great Lakes Symposium, 1993.
- Chairman, Indian Subcommittee, International Test Conference, 1983 and 1984.
- Session Chair: International Test Conference, 1984; IFIP Conference on AI in CAD, Tokyo, 1989; Fault-Tolerant Computing Symposium, 1990.
- Workshop Organizer: Computer Assisted Instruction at UNL (1973) and at IIT Kanpur, India (1974); Document Image Analysis at Lincoln (1994 and 1995).

- Over 30 invited talks at industrial research labs (AT&T Bell Labs, GTE, Tektronix, SCL-India, CNR-Italy, IBM Burlington, TI-India) and at universities in USA, Europe, and Asia.