CSCE 932: Fault Tolerance: Testing and Testable Design, Spring 2009

Tentative Schedule: 8:30-9:45, Tu and Th, Avery Hall, Room 352

Course Web Page: http://www.cse.unl.edu/~seth/932

Instructor: Sharad Seth, Avery Hall, Room 359 (seth@cse.unl.edu), Phone: 472-5003

Office Hours: I am flexible; send me a message whenever you need to see me and I will arrange to meet you at the earliest possible time. If this demand-driven scheduling does not work for you, let me know and I will schedule specific hours.

Prerequisites: Background in logic design and Boolean algebra plus some maturity in mathematics and CSE topics e.g. probability/statistics, discrete math, computer architecture and operating systems.

References: There is no single required textbook for this course. However, for the first part of the course, covering the background material in VLSI testing, you may consult one of several available textbooks:

1. Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing For Digital, Memory, & Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. N. K. Jha and S. Gupta, Testing of Digital Systems, Cambridge University Press, UK, 2003.
3. A. Miczo, Digital Logic Testing and Simulation, Second Edition, John Wiley, 2003

A more comprehensive list of sources appears on a separate sheet for handy reference.

Course Format: I will provide the necessary background on VLSI testing in the first part of the course. This material is well covered in the textbooks listed above. I will provide you with lecture overheads and notes but expect you to fill in the gaps on your own by referring to the textbooks and other sources. There will be several homework assignments devoted to this part.

For the rest of the semester we will delve into selected advanced topics of current research interest, biased toward my own interests in VLSI testing. The course format will change from lectures-by-me and discussion to presentations and discussions by every one in the class (I may come back to provide additional overview presentations on specific research topics.) Your presentations will be judged both on their contents and effective technical communication.

I will assist you in selecting a semester-long research project to work on. The project specification may well require multiple iterations therefore you should start thinking about it as soon as possible. The specification should be a proposal with two to three single-spaced pages of narrative along with a list of references that you plan to consult for the project.

At the beginning of your project work, you will carry out a comprehensive review of the background related to the project and document this in a written report of about 8-10 single spaced pages and a 30-minute oral presentation. I expect this to be completed by about 12th week of the semester.

For the research project, I expect original work that demonstrates your mastery of the topic. At its completion you will make another oral presentation and submit a paper-length written report (20-35 double spaced pages, including figures and references). The written report should include a brief literature review (3-5 pages), summarizing and possibly updating what you submitted earlier. It should follow the norms of good technical writing. Expect the final oral presentations to happen during the dead week and the written report to be due during the finals' week.

Grading:

Homework:		40%
Topical Presentations:		25%
Project:		
	Proposal and Presentation	15%
	Final Report and Presentation	20%

Conversion of Points to Letter Grades: The table below shows the letter grade corresponding to the total percentage score at or above the value indicated.

A+	A	A-	B+	B	B-	C+	C	C-	F
≥ 97	93	90	87	83	80	77	73	70	<70

Sources of Information in VLSI Testing and Testable Design

Textbooks:

1. Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing For Digital, Memory, & Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. N. K. Jha and S. Gupta, Testing of Digital Systems, Cambridge University Press, UK, 2003.
3. A. Miczo, Digital Logic Testing and Simulation, Second Edition, John Wiley, 2003.
4. L-T Wang, C-W Wu, X. Wen, VLSI Test Principles and Architectures: Design for Testability (Hardcover), Morgan Kaufmann; 1 edition (July 21, 2006).

The latest research in the field is published in the proceedings of conferences/workshops and journals. Almost all of this material is available online through iris.unl.edu. If you cannot find a paper, check with me; I have a large personal collection of papers on topics of interest to me. Here is a list of major non-textbook sources:

Conferences devoted to testing: International Test Conference (ITC), VLSI Test Symposium (VTS), European Test Symposium (ETS), Asian Test Symposium (ATS), IEEE International On-Line Testing Symposium (IOLTS).

Other conferences with significant test component: Design Automation Conference (DAC), International Conference on Computer Aided Design (ICCAD), International Conference on Computer Design (ICCD), VLSI Design Conference (VDC), Design Automation and Test in Europe (DATE), International Symposium on Circuits and Systems (ISCAS).

Journals devoted to testing or with significant test component: Journal of Electronic Testing: Theory and Applications (JETTA), IEEE Transactions on Computer Aided Design (TCAD), IEEE Transactions on Computers (TC), ACM Transactions on Design Automation of Electronic Systems (TODAES).

Organizations: The Test Technology Technical Committee (TTTC) is an active arm of IEEE devoted to organizing conferences, workshops and short courses. Through its website it disseminates information about the upcoming meetings and events of interest to test professionals. Other groups involved in test related activities include:

IEEE: Computer Society (CS) Circuits and Systems Society (CAS)
ACM: Special Interest Group on Design Automation (SIGDA)

Web Pages: Through your own resourcefulness you should be able to locate web pages of the leading research groups in VLSI testing across the globe. Also, there are online sources that maintain public-domain test tools and benchmarks. Links to some of these appear on the class web page.