

Course Announcement
CSCE 932, Spring 2009: Fault Tolerance
Call #: 8073, 3 Credit Hours
M, W, F: 11:30-12:20, AvH 111

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This offering of the course will take a broader view of fault tolerance in light of three trends in semiconductor manufacturing: (1) primacy of low-power issues in both high-volume and high-performance designs, (2) emergence of chip multiprocessors (CMPs) and novel on-chip interconnect structures, such as network-on-chip (NoC), to solve the technological issues of device integration and (3) the dynamic nature of the deep-submicron noise effects in the nanometer technologies.

We will discuss low-power and hot spot concerns that necessitate temperature-aware design-for-test techniques spanning multiple levels of abstraction, from algorithmic to register-transfer, to gate and circuit levels. We will discuss the rationale for packet-switching in CMPs for communication and the new testing problems introduced by the introduction on NoCs for packet-based communication. Finally, we will discuss techniques to combat *upsets* due to nano-technology, including online and concurrent testing.

The course will provide the necessary background in VLSI testing and exposure to test-related tools for in the first few weeks of the semester. Then we will delve into the current topics mentioned above, with the selection and depth determined by the background of students taking the course. The introductory material covered at the beginning can be found in any one of the many available textbooks, some of which can be found at the course website listed below. For the rest, we will be using journal and conference papers (available online from UNL Library), supplemented with papers from my own personal collection. The second part of the course will be seminar-style with active participation and contributions by students by way of individual presentations and projects.

The course should be of interest to CSE graduate students working in the systems area and to graduate students in EE working in the digital and communications areas. The formal prerequisite for the course is rudimentary understanding of VLSI design and knowledge of logic design and computer organization. The most important prerequisite, however, is an interest in the topics mentioned above and a curiosity to learn. If you have any questions about your preparation for the course, feel free to contact me by email or phone.

This announcement and any future updates about the course can be found at the course website: <http://cse.unl.edu/~seth/932/>.