lab 3 - place and route

Sina Balkir <sbalkir@unl.edu> **Tue, Oct 12, 2010 at 1:05 PM**
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There is one thing to keep in mind (hopefully only one) regarding lab 4. Lab 4 uses previously generated database files from previous labs. However, in lab 3, section V, the import stage of the synthesized controller failed to generate the schematic. While this will not be fixed, the students should still execute this stage. The reason is, when this import step is done, although the schematic generation fails, the system also generates a symbol view and a functional view. These symbol/functional views may come handy during lab 4, when symbols from lower hierarchies are called into the IC craftsman module for top level routing (lab 4 stuff). The functional view may also be used for verification at post layout stage maybe.

Anyway just wanted to remind you of this that during lab 3 this netlist import stage should still be done while LVS still fails due to lab 4 requirements, which is OK.

Note: Lab 4 uses IC craftsman which is the chip assembly router, if you follow the same file path conventions we adapted for our flow during labs 1-3, this lab 4 should normally work. Good luck.

--sina

> ----- Original Message -----
> **From:** Sharad Seth
> **To:** Sina Balkir
> [Quoted text hidden]