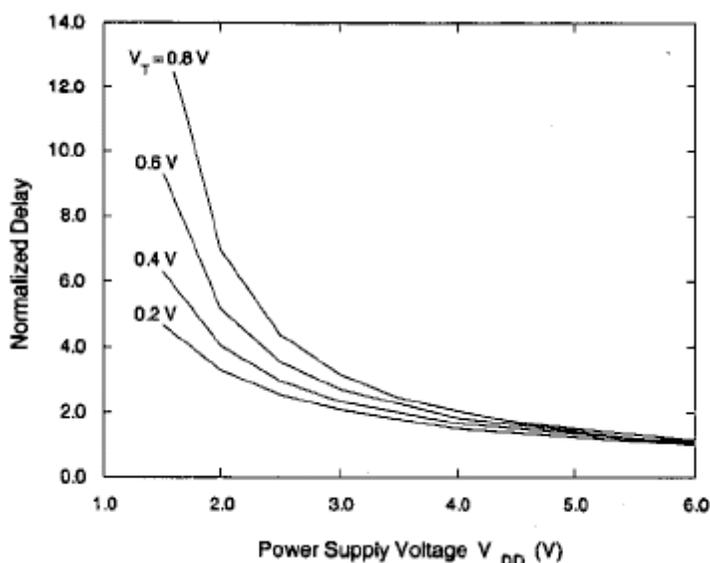


Homework 4 (Due October 25)

Note: Weights of problems are as indicated.

1. [20%] (a) The power consumption equation for CMOS circuits: $P = \alpha \cdot C \cdot V_{DD}^2 \cdot f$ indicates that if voltage is scaled down, the power consumption should go down quadratically. However, this analysis ignores the dependence of circuit speed on the power supply voltage. For example, the following graph shows the normalized delay of a CMOS inverter, as a function of the power supply voltage V_{DD} and the threshold voltage V_T .



(Fig. 11.10/p. 465 from Kang & Leblebici, *CMOS Digital Integrated Circuits*)

Taking this dependence into account, is the reduction in power stronger or weaker than quadratic? Provide a complete justification for your answer.

(b) Extending the above argument, what can you say about the total energy consumption in the CMOS circuit to carry out the same computation, with and without voltage scaling, i.e. indicate the order-of-magnitude (big-oh) dependence of the energy consumption on voltage scaling, along with a justification for your answer.

2. [20%] We know that there is a tradeoff between energy consumption and delay in a CMOS circuit. This problem explores this tradeoff quantitatively for the case of driving a large load through a chain of inverters. Assume the total electrical effort (i.e. the ratio of output to input capacitance) is 1000 and the load is driven through an odd number N of inverters sized to achieve optimum delay for the given number inverter stages. Plot the power vs. delay curve by considering $N = 1, 3, 5, 7,$ and 9 and comment on your result.

3. [30%] Consider the full-adder design shown in Fig. 11.3/page 431 of the textbook. It makes use of five CMOS gates (three inverters at the input, the sum gate, and the carry gate).

(a) Assume the transistors in the two complex gates are sized to have the pull-up and pull-down resistance equivalent to a unit inverter. Determine and show the sizes of all the transistors. Then compute the logical effort for each gate input and the parasitic delay of each gate.

(b) Next, assume that the adder design has been augmented with an additional stage of inverter at each input and output (which does not change the function of the circuit) and that both the sum and the carry outputs drive a load equivalent to FO-4 inverter. Using the iterative method for sizing gates discussed in the class (you may also refer to Sections 4.5.6 and 5.2.2.1 of the textbook) determine the energy consumption, the delay, and the gate sizes of the full adder, when the gates are sized to minimize the delay through the circuit. Show all calculations. *Note that the energy and the delay must be normalized with respect to a unit inverter. You may assume that all inputs to the adder have a 1-probability of 0.5.*

(c) Next, consider reducing the energy consumption by allowing the delay to range between D_{\min} and $3 \cdot D_{\min}$, where D_{\min} is the minimum delay you obtain in part (b). Divide the delay interval, roughly, into 8 points and for each point compute the minimum energy consumption and gate sizes. Show the results in a table with one row for each point, showing the delay, the power, and the gate sizes. Also, show a plot of energy vs. delay.

4. [15%] Consider, again, the full-adder design as in Problem 3(b) but assume a *non-uniform* distribution of input signal probabilities. Specifically, assume that:

$$P_A = 0.3, P_B = 0.2 \text{ and } P_C = 0.6$$

Compute the signal probability and the activity factor at the output of each gate and show your results on a logic schematic of the circuit.

5. [15%] Problem 5.1 from the textbook.