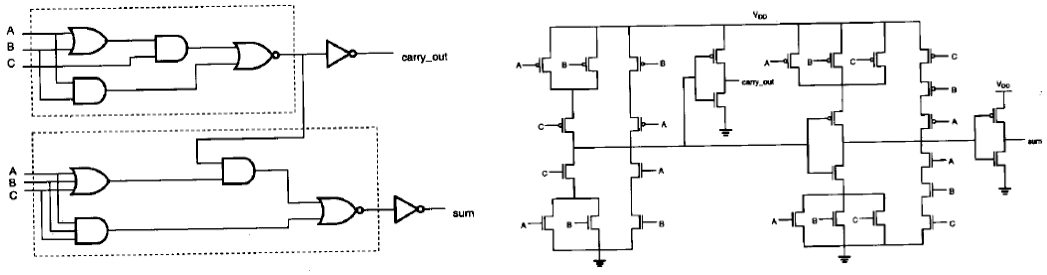
CSCE 434/834, Fall 2010

Homework 3 (Due October 8)

Note: Weights of problems are as indicated.

1. [40%] The logical and CMOS schematics of a full-adder implementation are shown below:



Note that the implementation uses two complex CMOS gates and two inverters.

(a) Assume, all gates are minimum size allowed by the SCMOS technology we have discussed in the class. For each complex CMOS gate:

- Compute the parasitic delay, expressed in *lambda units* for the output diffusion area
- Compute the logical effort for every input to the gate, expressed in the units of the logical effort of the fanout-of-1 inverter (*FO-1 inverter*) shown in Fig. 4.6 of the textbook.

Provide brief justifications for your answers.

(b) Assume that the transistors in each complex gate are sized so that the unloaded rise and fall times are equivalent to that of an FO-1 inverter. Show the transistor sizes on the schematics of each complex gate, then compute the parasitic delay of the gate and the logical effort at each gate input, both expressed in terms of an FO-1 inverter.

(c) Assume the load on the sum output is equal to that offered by 64 FO-1 inverters and the load at the A input of each complex gate is equal to one FO-1 inverter. Size the two complex gates such that the delay from the A input of the top CMOS gate to the sum output is minimized. Show all calculations.

Problem 2. [10%] Ex. 4.7 from the textbook.

Problem 3. [20%] Ex. 4.12 from the textbook.

Problem 4. [15%] Ex. 4.15 from the textbook.

Problem 5. [15%] Ex. 4.16 from the textbook.