CMOS VLSI Design 4e vs. 3e

The following table shows the rough correspondence between the new (4e) and the old (3e) editions of the book by Weste and Harris). On Amazon.com the two editions sell for approximately the same price and since the new edition updates the old 2004 publication, you should definitely consider buying the new editions

4th Ch	3rd Ch	Short Title	Comments
1	1	Introduction	Almost same.
2	2	MOS Theory	4e excludes §2.6 Switch-level RC Delay Models
3	3	Fab Process	Same
4-7	4	Performance	Old chapter on Circuit Characterization and Performance (108 pp) has been split into four new chapters with enhancements (140 pp) on Delay, Power, Interconnect, and Robustness
8	5	Ckt Simulation	Almost same
9	6	Comb Logic	Almost same
10	7	Seq Logic	Essentially unchanged except the old optional section §7.5 on Sequencing Dynamic Circuits has move to the Web.
11	10	Datapath	Same
12	11	Arrays	Same except old §11.8 (1 p) on Array Yield, Reliability, and Self-test has been expanded to 3 pages on Robust Memory Design
13	12	Special Purpose Subsystems	Old §12.6 on Analog Circuits (amps, current mirrors, diff. pairs, op-amps, DAC, ADC, and RFC) comprising c. 30 pages has been removed in favor of the new §13.5 on PLLs, DLLs. Also, there are new sections §13.7 on High-speed Links, and §13.8 on Random Circuits
14	8	Design Methods & Tools	First six sections (c. 40 pages) are essentially the same. Old §8.8 (CMOS Physical Design Styles) has been moved to the Web and the following old sections have been dropped: §8.7 (Closing the Gap Between ASIC and Custom), §8.9 (Interchange Formats), and §8.10 (Historical Perspective)
15	9	Testing etc.	Old §9.7 Boundary Scan has been moved to the Web and the following old sections have been dropped: §9.8 (SoC Testing), §9.9 (Mixed Signal Testing), and §9.10 (Reliability Testing)
App A	Apps A &B	HDL	The old appendices, split along Verilog and VHDL, have been combined into a single appendix on HDLs.