

CSCE 230, Spring 2012 Tentative Course Schedule

Note: The actual schedule may differ from the following in details, to accommodate unforeseen circumstances. The schedule shows integration of course material with the lab assignments in CSCE 230L.

Wk.	Material Covered	Assignment	Tests
1	“Startup” to course, course overview, Ch. 1.	Lab #1: Introduction to Altera DE1 boards: hardware and software.	
2	Instruction set architecture (Ch. 2.1–2.5 & App. B)	Lab #1: (continued)	
3-4	Instruction set architecture (Ch. 2.6–2.13 & App. B)	Lab #2: Introduction to NiosII assembly language. Lab #3: Assembly language programming: arrays, loops, and procedures.	
4-5	Basic input-output (Ch. 3 & App. B.9–B.11)	Lab #4: Assembly language programming: recursion and stack.	Test 1 (Chs. 1 and 2)
6	Software (Ch. 4)	Lab #5: Basic I/O programming using busy waiting and interrupts. Project specification out. Team work continues to the end of the semester.	
7	Logic design (App. A.1–A.4, A.5.2–A.5.4, A.6.1–A.6.2)	Lab #6: Logic design exercise 1	
8	Logic design (App. A.6.3, A.6.4, A.7–A.10, A.12–A.13)	Lab #7 Logic design exercise 2	
9	Basic processing unit (Ch. 5.1–5.4)	Lab #8 Logic design exercise 3	Midterm (Chs. 3, 4, App. A)
10	Basic processing unit (Ch. 5.5–5.7)	Lab #9 Logic design exercise 4	
11	Pipelining (Ch. 6)	Project work	
12	Input-output organization (Ch. 7.1–7.4, selected topics from 7.5)	Project work	
13	The memory system (Ch. 8.1–8.6, omitting bit-cell details)	Project work	Test 2 (Chs. 5, 6, & 7)
14	The memory system (Ch. 8.7–8.10)	Project work	
15	(Time permitting) Arithmetic (Ch. 9 – selected parts)	Project work. Oral presentations may start during the dead week and continue to finals’ week.	
16		Project report – oral and written	Final (at scheduled time)

Homework: There will be about 8 assignments, each related to the material covered in a chapter or appendix.