Due: November 9, 2015

Name (Last, First): Solution Key

CSCE 230, Fall 2015
Homework 5

Notes:

- **This assignment must be typed.** Assignments which are not typed will not be graded.
- A hard copy **and** an electronic copy must be submitted by the beginning of class on the due date.
- Staple this coversheet to your completed assignment.

Material Covered:

Appendix A

Chapter 9

Chapter 5

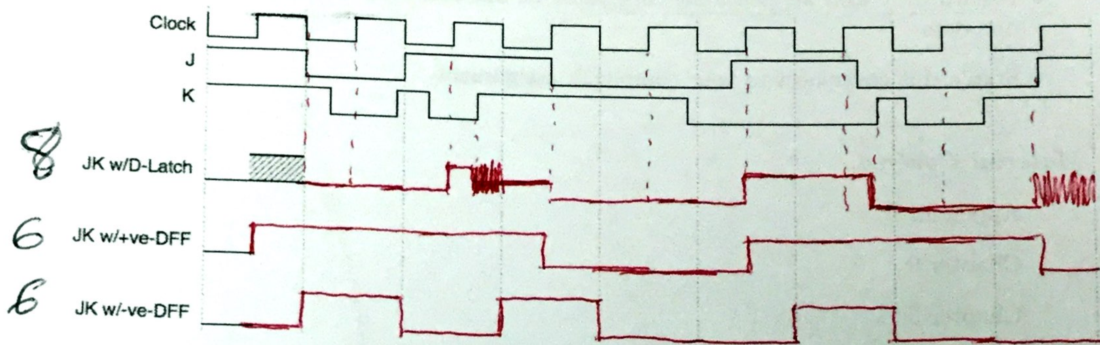
Rubric:

Problem Number	Possible Points	Points Earned
1	20	100
2	30	100
3	20	100
4	20	100
5	10	100
6	10	100
	Total:	600

Problem 1 [20]

Topic: *JK Flip-Flop*

JK flip flops combine the behaviors of D and T flip flops, and can be implemented using a rising edge D flip flop or using D Latches and falling edge D flip flops. After reviewing Section A.6.5 and Section A.13.2 in your book, use the input waveform below to draw the output waveforms for each of the following JK flip flop implementation.



Problem 2 [30]

Topic: *Finite State Machine*

Using FSM design principles, design a vending machine. The vending machine accepts quarters or dimes – so a one-bit input variable can be used to model the type of coin. One product is available in the machine. The output is a one-bit variable that is 0 if the amount of money deposited is not insufficient and is 1, otherwise. The product costs 50 cents. In each clock cycle, the user can drop a single coin (quarter or dime). No changes or refunds are provided. State any assumptions you may make.

a) List the possible states of the vending machine. The machine should have at least one state (START) that represents the case when no coins are dropped and one state (END) that represents the case when enough money is deposited. You can simplify the design by designing such that any value equal to or above 50 cents transitions to the same END state. You will need to consider the combinations of quarters and dimes that lead to 50 cents or more to find the other states.

b) Draw the state diagram similar to Figure A.46. The machine should always transition from the END state to the START state (when the product is deposited, machine goes back to the initial state). Use labels for state names.

c) Using the state diagram, show the state table similar to Figure A.47.

d) Based on the number of states, find the number of bits required and assign bit values to each state. Show the updated state table similar to Figure A.48.

e) Find the logic representation of next state and output variables as a function of current state and input variables.

f) Draw the logic implementation similar to Figure A.49 (larger number of flip flops may be required).

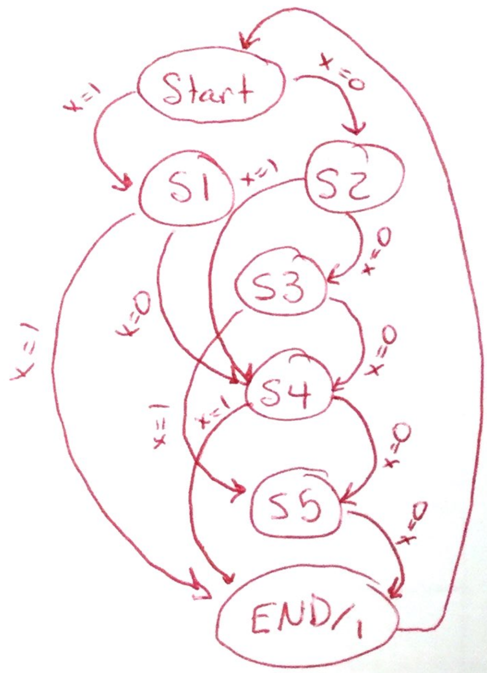
2.

a) States

Start
1 dime
2 dimes
1 quarter
1 quarter, 1 dime ⇔ 3 dimes
1 quarter, 2 dimes ⇔ 4 dimes
End

5 pts / subquestion

b)



c)

Current State	Next State x=0	Next State x=1	Z
S0	S2	S1	0
S1	S4	S6	0
S2	S3	S4	0
S3	S4	S5	0
S4	S5	S6	0
S5	S6	S6	0
S6	S0	S0	1

d)

Current State	Next State x=0	Next State x=1	Z
000	010	001	0
001	100	110	0
010	011	100	0
011	100	101	0
100	101	110	0
101	110	110	0
110	000	000	1
	xxx	xxx	0
$Y_1 Y_2 Y_3$	$y_1 y_2 y_3$	$y_1 y_2 y_3$	

e) $Y_1 = \overline{Y_1}\,\overline{Y_2}Y_3\overline{X} + \overline{Y_1}\,\overline{Y_2}Y_3X + \overline{Y_1}Y_2\overline{Y_3}X + \overline{Y_1}\,\overline{Y_2}Y_3\overline{X}$
$+ \overline{Y_1}Y_2Y_3X + Y_1\overline{Y_2}\,\overline{Y_3}\overline{X} + Y_1\overline{Y_2}\,\overline{Y_3}X + Y_1\overline{Y_2}Y_3\overline{X} + Y_1\overline{Y_2}Y_3X$

Y_3X \ Y_1Y_2	00	01	11	10
00				
01	1	1	1	1
11	1		x	
10	1	1	1	1

$Y_1 = \overline{Y_3}X + Y_3\overline{X} + \overline{Y_1}\,\overline{Y_2}X = Y_3 \oplus X + \overline{Y_1}\,\overline{Y_2}X$

$Y_2 = \overline{Y_1}\,\overline{Y_2}\,\overline{Y_3}\,\overline{X} + \overline{Y_1}\,\overline{Y_2}Y_3X + \overline{Y_3}Y_2\overline{Y_3}\,\overline{X} + Y_1\overline{Y_2}\,\overline{Y_3}X + Y_1\overline{Y_2}Y_3\overline{X}$
$+ Y_1\overline{Y_2}Y_3X$

Y_3X \ Y_1Y_2	00	01	11	10
00	1			
01		1		
11	1		x	1
10		1	x	1

~~$Y_2 = Y_1Y_3X + Y_1\overline{Y_2}Y_3 + \overline{Y_1}\,\overline{Y_2}\,\overline{Y_3}\,\overline{X} + \overline{Y_1}Y_2\overline{Y_3}X + \overline{Y_1}\,\overline{Y_2}Y_3X + \overline{Y_1}Y_2Y_3\overline{X}$~~

$Y_2 = Y_1Y_3 + Y_2Y_3\overline{X} + \overline{Y_2}Y_3X + \overline{Y_1}\,\overline{Y_2}\,\overline{Y_3}\,\overline{X} + Y_1Y_2\overline{Y_3}X$

$Y_1 = \bar{Y}_1 \bar{Y}_2 Y_3 \bar{x} + \bar{Y}_1 \bar{Y}_2 Y_3 x + \bar{Y}_1 Y_2 \bar{Y}_3 x + \bar{Y}_1 \bar{Y}_2 Y_3 \bar{x}$

$+ \bar{Y}_1 Y_2 Y_3 x + Y_1 \bar{Y}_2 \bar{Y}_3 \bar{x} + Y_1 \bar{Y}_2 \bar{Y}_3 x + Y_1 \bar{Y}_2 Y_3 \bar{x} + Y_1 \bar{Y}_2 Y_3 x$

Y_3x \ Y_1Y_2	00	01	11	10
00				
01	1	1	1	1
11	1			
10	1	1	1	1

$Y_1 = \bar{Y}_3 x + Y_3 \bar{x} + \bar{Y}_1 \bar{Y}_2 x = Y_3 \oplus x + \bar{Y}_1 \bar{Y}_2 x$

$Y_2 = \bar{Y}_1 \bar{Y}_2 \bar{Y}_3 \bar{x} + \bar{Y}_1 \bar{Y}_2 Y_3 x + \bar{Y}_3 Y_2 \bar{Y}_3 \bar{x} + Y_1 \bar{Y}_2 \bar{Y}_3 x + Y_1 \bar{Y}_2 Y_3 \bar{x}$

$+ Y_1 \bar{Y}_2 Y_3 x$

Y_3x \ Y_1Y_2	00	01	11	10
00	1			
01		1		
11	1		X	1
10		1	X	1

~~$Y_2 = Y_1 Y_3 x + \ldots$~~

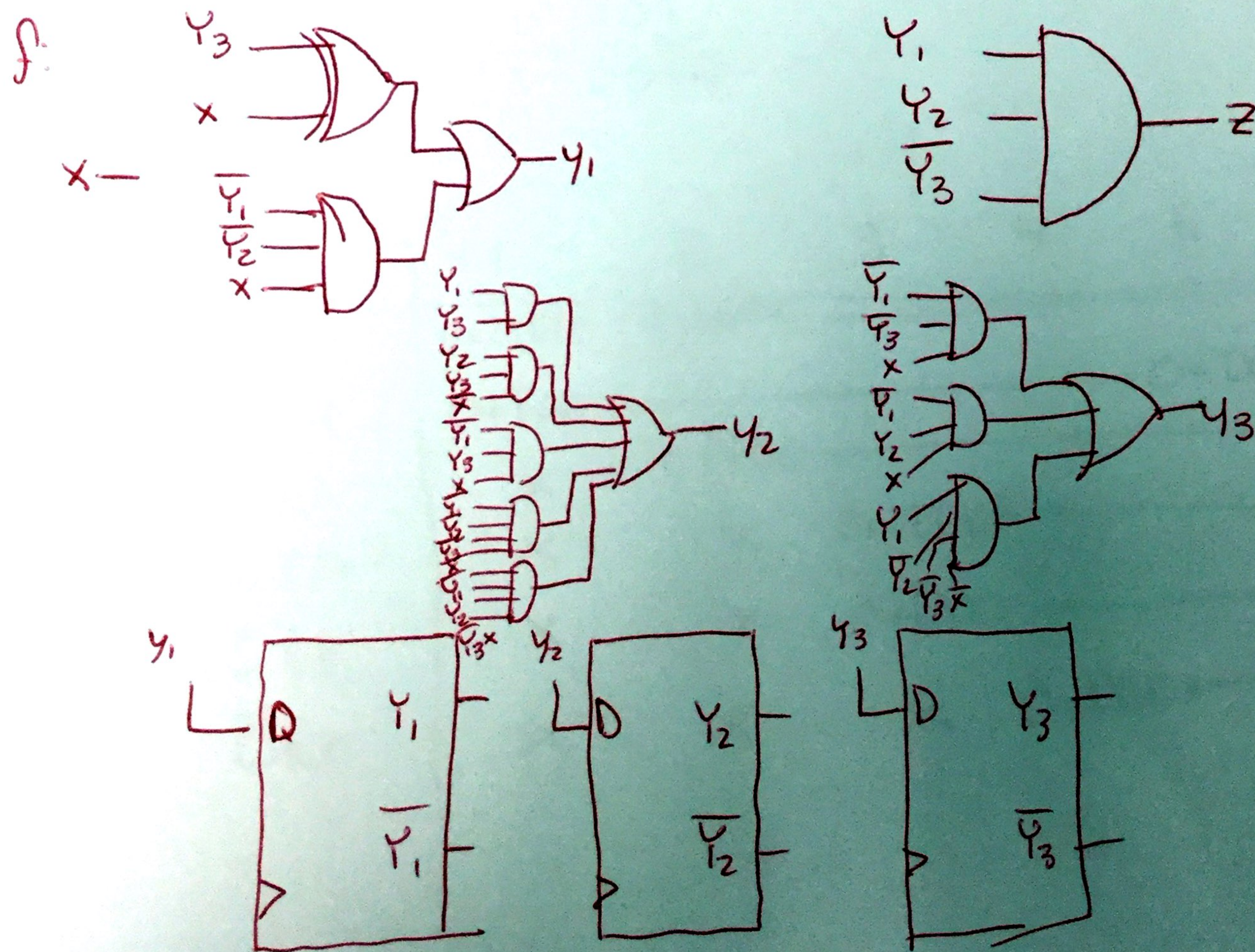
$Y_2 = Y_1 Y_3 + Y_2 Y_3 \bar{x} + \bar{Y}_2 Y_3 x + \bar{Y}_1 \bar{Y}_2 \bar{Y}_3 \bar{x} + \bar{Y}_1 Y_2 \bar{Y}_3 x$

$$Y_3 = \overline{Y_1}\,\overline{Y_2}\,\overline{Y_3}x + \overline{Y_1}Y_2\overline{Y_3}x + \overline{Y_1}Y_2Y_3x + Y_1\overline{Y_2}\,\overline{Y_3}\,\overline{x}$$

Y_3x \ Y_1Y_2	00	01	11	10
00	0			1
01	1	1		
11		1	X	
10			X	

$$Y_3 = \overline{Y_1}\,\overline{Y_3}x + \overline{Y_1}Y_2x + Y_1\overline{Y_2}\,\overline{Y_3}\,\overline{x}$$

$$Z = Y_1Y_2\overline{Y_3}$$



3 a:

```
       10101
     × 00101
     -------
       10101
  +   000000
  +  1010100
  + 00000000
 + 000000000
 -----------
  001101001
```

$001101001_2 = 105_{10}$

10 pts

b:

```
          100.00100
101 ) 10101.000000
     -101
      001000
     -   101
      ------
         110
         101
        ----
        0010
```

10 pts

4:

	Stage:	1	2	3	4	5	1
4	PC	0x21DF0	0x21DF4 →	→	→	→	→
4	R4	0xF00 →	→	→	→	0xD00 →	→
4	RA	×	0xF00 →	→	→	→	→
2	RM	×	×	0x02D05 →	→	→	→
2	RZ	×	×	0xD00 →	→	→	→
2	RY	×	×	×	0xD00 →	→	→

5: A comparator in the form of a subtractor must be placed in step 2. 5pts Branches must be done after the compare. 5pts

6: First, the addition is done in stage 3, and loading is done in stage 4. Next, Only one immediate value can be used (Ø for the address, 4 for the increment.). Next, Only one value can be placed into RY, either the memory result or the ALU result, not both. Lastly, only one register can be written to in an instruction. Any one of these makes an okay answer. + 10 if any is mentioned