Analyzing the Real-Time Properties of a Dataflow Execution Paradigm using a Synthetic Aperture Radar Application*

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Abstract

Real-time signal processing applications are commonly designed using a dataflow software architecture. Here we attempt to understand fundamental real-time properties of such an architecture — the Navy's coarse-grain *Processing Graph Method* (PGM).

By applying recent results in real-time scheduling theory to the subset of PGM employed by the ARPA RASSP Synthetic Aperture Radar benchmark application, we identify inherent real-time properties of nodes in a PGM dataflow graph, and demonstrate how these properties can be exploited to perform useful and important system-level analyses such as schedulability analysis, end-to-end latency analysis, and memory requirements analysis. More importantly, we develop relationships between properties such as latency and buffer bounds and show how one may be traded-off for the other. Our results assume only the existence of a simple EDF scheduler and thus can be easily applied in practice.

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1 Introduction

Signal processing algorithms are often defined in the literature using large grain dataflow graphs [12]: directed graphs in which a node is a sequential program that executes from start to finish in isolation (i.e., without synchronization), and the graph edges depict the flow of data from one node to the next. Thus, an edge represents a producer/consumer relationship between two nodes. Large grain dataflow provides a natural description of signal processing applications with each node representing a mathematical function to be performed on an infinite stream of data that flows on the arcs of the graph. The streams of input data are typically generated by sensors sampling the environment at periodic rates and sending the samples to the signal processor via an external channel. The dataflow methodology allows one to easily understand the signal processing performed by depicting the structure of the algorithm; any portion of the application can be understood in the absence of the rest of the algorithm.

Embedded signal processing applications are naturally defined using dataflow techniques. As real-time applications, they require deterministic performance. The signal processing graph must process data at the rates of a set of external devices (e.g., sonobuoys, dipping sonars, or radars) without the loss of data. Hence signal processing applications, like other real-time systems, have a dual notion of correctness: logical and temporal. It is not sufficient to only produce the correct output — e.g., the signature of a detected target; embedded signal processing applications must produce the correct output within the correct time interval — e.g., detect the signature within 1 second.

Dataflow models implicitly define a temporal semantics for a processing graph by specifying lower bounds on when nodes may execute as a function of the availability of data on input edges. However, most models do not support the specification of either an end-to-end latency constraint or an upper bound on the time that may elapse between when a node becomes eligible to execute and the time the node either commences or completes execution. Without one of these specifications, we are left with:

- no schedulability or admission control test — How does one determine if a set of nodes or a graph "fits" on a processor?
- undetermined latency properties — How does one determine if a graph meets its timing requirements?
- no upper bound on queue length — If latency is not bounded, memory requirements for a graph cannot be bounded and hence data loss may occur if enough storage is not provided.

System engineers use such metrics to size hardware and perform requirements verification. A cost trade-off may be made on CPU utilization versus latency, or buffer space versus latency. High latency tolerances allow the use of a slower (and cheaper) CPU but may require more memory for increased buffer space. On the other hand, tighter latency requirements may demand a faster CPU (or lower utilization) but less memory. In keeping costs in line, a system architect uses these metrics to make fundamental design trade-offs.

Unfortunately, without the application of real-time scheduling theory to dataflow methodologies and a precise execution model, system architects have not been able to make these trade-offs in real-time dataflow systems. Even the Navy's own dataflow methodology, *Processing Graph Method* (PGM) [16], lacks real-time analysis techniques to support making cost trade-offs or to verify latency requirements. This is somewhat

surprising since PGM is used to develop real-time, embedded, anti-submarine warfare (ASW) applications for the AN/UYS-2A (the Navy's standard signal processor). PGM has also been used to create a real-time Ka-band synthetic aperture radar (SAR) benchmark application for ARPA's Rapid Prototyping of Application Specific Signal Processors (RASSP) project.

In this paper, we present a novel application of real-time scheduling theory to the subset of PGM used in the RASSP SAR benchmark application. Using the SAR application graph as a driving problem, we identify inherent relationships existing in real-time dataflow that have not been recognized in the literature. We present theorems that characterize the non-trivial execution rates of every node in the dataflow graph as a function of input rates by applying existing real-time scheduling theory to the dataflow methodology. From scheduling theory, we get a scheduling condition for preemptive earliest deadline first (EDF) scheduling algorithms. If the scheduling condition returns an affirmative result, the graph can be scheduled (with a preemptive EDF algorithm) to meet specified execution deadlines. We also show how to set the deadline parameters to bound end-to-end latency and memory requirements.

The rest of this paper is organized as follows. Our results are related to other work in Section 2. Section 3 presents a brief overview of the portion of PGM used by the SAR graph, which is introduced in Section 4. Section 5 presents node execution rates and a schedulability condition for EDF scheduling. Section 6 addresses latency issues and Section 7 shows how to bound the buffer requirements of an implementation of a graph. We summarize our contributions in Section 8.

2 Related Work

This research was inspired by the analysis techniques applied to three different dataflow models: the dataflow graphs found in the Software Automation for Real-Time Operations (SARTOR) project led by Mok [14, 15], Lee and Messerschmitt's Synchronous Dataflow (SDF) graphs [12] supported by the Ptolemy system [4], and the Real-Time Producer/Consumer (RTP/C) paradigm of Jeffay [8]. Unfortunately, none of these paradigms (or any other dataflow paradigms from the literature) correctly model the execution of PGM graphs.

The dataflow graphs of the SARTOR project have different (and incompatible) node execution rules from PGM. As with the SARTOR project, our goal is to demonstrate that we can apply real-time scheduling results to real-life applications.

Like the RTP/C paradigm, we use the structure of the graph to help specify execution rates of the processes. However, our execution model is capable of supporting much more sophisticated data flow models than RTP/C. Whereas RTP/C models processes as sporadic tasks, our paradigm uses the Rate-Based Execution (RBE) process model of [10] to more accurately predict processor demand. (The RBE process model is a generalization of sporadic tasks and the Linear-Bounded Arrival Process (LBAP) model employed by the DASH system [1].) Unlike the RTP/C paradigm, PGM supports *And* nodes (nodes that are eligible to execute only when all of the input queues are over threshold), which introduces different execution properties than those of the RTP/C paradigm.

The SDF graphs of Ptolemy utilize a subset of the features supported by PGM. In addition to supporting

a more general dataflow model, our research differs from [12] in that we use dynamic, real-time, scheduling techniques rather than creating static schedules.

Our latency analysis is related to the work of Gerber et al. in guaranteeing end-to-end latency requirements on a single processor [6]. Our work differs from [6] in that we cannot assume a periodic task model and that our node execution rates are derived from the input data rate and the graph. Moreover, unlike [6], we do not introduce new (additional) tasks for the purpose of synchronization.

3 Dataflow Model

This section describes the features of PGM used in the SAR graph. For a complete description of PGM, see [16].

In PGM, a system is expressed as a directed graph of large grain nodes (processing functions) and edges (logical communication channels). The topology of the graph defines the flow of data from an input source to an output sink, defining a software architecture independent of the hardware hosting the application. The edges of a graph are typed First-In-First-Out (FIFO) queues. The data type of the queue indicates the size of each token (a data structure) transported from a producer to a consumer. Tokens are appended to the tail of the queue (by the producer) and read from the head (by the consumer). The tail of a queue can be attached to at most one node at any time. Likewise, the head of a queue can be attached to at most one node at any time.

There are three attributes associated with a queue: a produce, threshold, and consume amount.[1] The produce amount specifies the number of tokens atomically appended to the queue when the producing node completes execution. The threshold amount represents the minimum number of tokens required to be present in the queue before the node may process data from the input queue. The consume amount is the number of tokens dequeued (from the head of the queue) after the processing function finishes execution. A queue is *over threshold* if the number of enqueued tokens meets or exceeds the threshold amount. Unlike many dataflow paradigms, PGM allows non-unity produce, threshold, and consume amounts as well as a consume amount less than the threshold. The only restrictions on queue attributes is that they must be non-negative values and the consume amount must be less than or equal to the threshold. For example, a queue may have a produce of 2, a threshold of 5, and a consume of 3.

Although PGM supports general graphs consisting of nodes with multiple input queues and variable produce and consume values, the SAR graph does not use these features. Since our driving application has the topology of a chain of nodes, for space consideration we restrict our analysis to chains and simply note that all of the results presented in this paper can be extended to general PGM graphs.

[1] In PGM, a produce, threshold, or consume attributes is associated with a node port rather than the queue. For the subset of PGM used by the SAR application, it is easier to associate these attributes with the queue rather than the node.

4 SAR Graph

This section introduces the SAR graph including a brief description of the processing performed by each node in the graph. This information is provided for concreteness for the reader with a signal processing background. The actual logical operation of the SAR graph is immaterial to the results we derive and the analyses we perform. The only essential properties of the SAR graph are those that influence node execution: the produce, consume, and threshold values for each node. For a more detailed description of the processing performed by the SAR benchmark, see [17].

The full SAR benchmark cannot execute in real-time on a single processor. Therefore, the RASSP project allocates a portions of the full SAR graph to individual processors. The graph in Figure 1 is one such allocation. This graph, called the "mini-SAR", was originally created to test tools developed by the RASSP project. It performs the range and azimuth compression processing in the formation of an image that is one eighth the size of that formed by the full SAR benchmark. Henceforth, we shall refer to the mini-SAR graph as the SAR graph since an analysis similar to what we develop shortly, could be performed on each processor to analyze the full application.

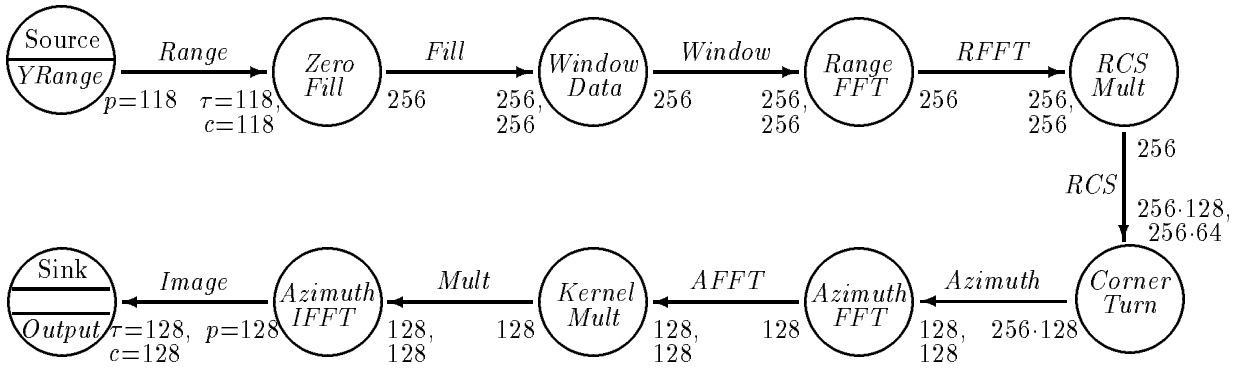


Figure 1: SAR Graph

The source node for the SAR graph (shown in Figure 1) is labeled *YRange* and represents a periodic external device that produces data for the graph. The sink node, represents an external device that executes whenever data is available on the *Image* queue. The nodes and queues of this graph have mnemonic labels. (For a generic chain, we would label the source node N_0 and the sink node N_{n+1}. The output queue for node N_i would be labeled Q_i.) Produce, threshold, and consume values are annotated below the queue. For example, the produce, consume, and threshold values of the queue labeled *Range* are all 118.

The top row of nodes in the SAR graph each operate on one pulse of data at a time. The pulse delivered by the external source, labeled *YRange*, has already been converted to complex-valued data and consists of 118 range gate samples. The *Zero Fill* node pads the pulse with zeroes to create a pulse length of 256 samples in preparation for the *FFT* node. Before performing the FFT, the data is passed through a Kaiser window function, represented by the node *Window Data*, to reduce sidelobe levels and perform bandpass filtering. After being compressed in the range dimension by the *Range FFT* node, the pulse is passed through the

radar cross section calibration filter performed by the *RCS Mult* node.

Unlike the previous nodes in the SAR graph, which require only one pulse of data before being eligible for execution, the *Corner Turn* node requires 128 pulses of data. A 2-D processing array is formed where each row of the array contains one sample from the 128 different pulses and each column contains the 256 range gates that form a pulse. The processing array consists of two 64×256 frames (or sequences of pulses). As a new frame is loaded in, the previous two frames are "released" with the oldest frame being shifted out. This processing is achieved with threshold and produce values of $256 \cdot 128$ and a consume value of $256 \cdot 64$.

Convolution processing is performed on each row of the 2-D matrix by the *Azimuth FFT*, *Kernel Mult*, and *Azimuth IFFT* nodes. The *Azimuth FFT* node performs a FFT on the signal, which has been aligned in the azimuth dimension. Next the *Kernel Mult* node multiplies each row of the matrix by a convolution kernel. Before the SAR image is output to the *Sink* node, an inverse FFT is performed by the *Azimuth IFFT* node.

5 Execution Model

Real-time scheduling theory provides a framework upon which we have developed an execution model that supports bounding latency and memory usage for PGM graphs. These bounds in turn can be used to guarantee no data loss occurs during graph execution. We also appeal to scheduling theory to provide guarantees that these bounds will be met without the need to check for violations during graph execution (assuming the basic assumptions made during the analysis phase are true at run-time).

This section introduces an execution paradigm and analysis techniques that support the evaluation of real-time properties for a graph. The first subsection explores fundamental execution relationships that exist between producer/consumer nodes, independent of the execution model. The remaining subsections address node execution rates and the RBE task model. These concepts are used to model an implementation of the graph.

5.1 Node Executions

Before exploring the fundamental execution relationships that exist between producer/consumer nodes, we must first define the restrictions on node execution. In accordance with PGM, our execution model requires all of the input queues to a node to be over threshold before the node is eligible for execution. Standard practice in implementing dataflow systems ([8, 12, 15]), though not part of the PGM specification, is to disallow two overlapping executions of the same node; we have adopted this restriction. PGM also requires that data be read from an input queue at the beginning of node execution, but data is consumed after the node has produced data on its output queues, which simply makes it clear that a node requires simultaneous input and output buffer space. We add the common real-time dataflow restriction that no data loss can occur during graph execution. The following definitions provide a formal basis for discussing the execution of nodes.

Definition 5.1. Queue Q_i is *over threshold* when it contains at least τ_i tokens, where τ_i is the threshold dataflow attribute of the queue.

Definition 5.2. Node N_i is *eligible for execution* when all of its input queues are over threshold.

Definition 5.3. The execution of a node is *valid* if and only if:

- the node executes only when it is eligible for execution,
- no two executions of the same node overlap,
- each input queue has its data atomically consumed after each output queue has its data atomically produced, and
- data is produced at most once on an output queue during each node execution.

Definition 5.4. *Graph execution* consists of executing a (possibly infinite) sequence of nodes from the set of nodes in the graph.

Definition 5.5. The execution of a graph is *valid* if and only if all of the nodes in the execution sequence have valid executions and no data loss occurs.

We introduce the execution relationship that exists between producer/consumer nodes using three different producer/consumer pairs of nodes and the results of different dataflow attributes on their adjoining queue. Unlike the SAR graph, Example 5.1 contains queues whose produce and threshold values are relatively prime — this is done to illustrate the general relationships between dataflow attributes and node execution. In each produce/consumer pair of Example 5.1, Q_i is annotated with its produce, threshold, and consume values below the queue.

Example 5.1. In the two node chain of Figure 2, N_i produces 2 tokens every time it executes. N_{i+1} has a threshold of 7 and consumes 7 after it executes. Since each execution of N_i produces 2 tokens, 4 executions

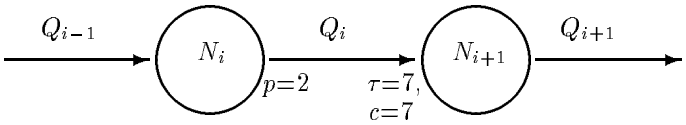


Figure 2: $Chain_1$

of N_i are required to complete before the first execution of N_{i+1} occurs. When N_{i+1} executes, it consumes 7 of the 8 tokens on Q_i, hence, only 3 additional executions of N_i (producing 6 more tokens for a total of 7 on Q_i) are needed for N_{i+1} to execute a second time. After N_{i+1} executes the second time, it consumes all 7 tokens on Q_i leaving it in the same state as we began, with 0 tokens. If we followed subsequent executions, we would find that the number of executions required of N_i to produce enough data for N_{i+1} to execute continues to alternate between 4 and 3. Therefore, 7 executions of N_i tokens will produce 14 tokens and result in N_{i+1} executing twice. What happens when the produce amount is greater than the threshold? Changing our two node chain so that N_i produces 7 and N_{i+1} has threshold and consume values of 2, as in

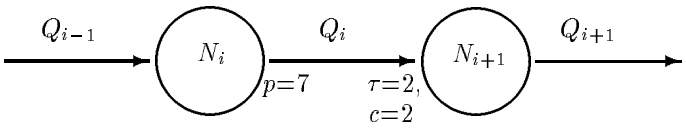


Figure 3: $Chain_2$

Figure 3, results in the first execution of N_i enabling 3 executions of N_{i+1} and the second execution of N_i enabling 4 executions of N_{i+1}. This is because the first 3 executions of N_{i+1} left 1 token on Q_i. After 2 executions of N_i and the resulting 7 executions of N_{i+1}, Q_i is left in its original state: containing 0 tokens.

Finally, consider the two node chain of Figure 4. N_i produces 4 tokens every time it executes. N_{i+1} has a

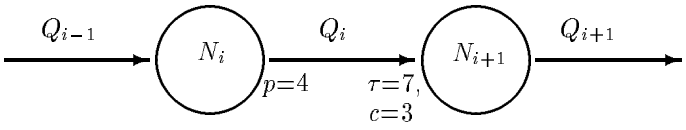


Figure 4: $Chain_3$

threshold of 7 and consumes 3 after it executes. Consequently, N_i must fire twice before Q_i is over threshold and N_{i+1} executes for the first time. After N_{i+1} executes, it consumes only 3 tokens — leaving 5 tokens on Q_i. The third execution of N_i produces 4 more tokens (for a total of 9 tokens on Q_i) and N_{i+1} executes again, consuming 3 more tokens. The next execution of N_i results in 10 tokens on Q_i, and N_{i+1} is able to execute twice — leaving 4 tokens on Q_i, which is the same number that were on Q_i after the first execution of N_i. Hence, subsequent executions of N_i and N_{i+1} follow this same pattern. □

Example 5.1 demonstrates that the number of tokens on Q_i at time t is a function of the the queue's dataflow attributes and the number executions of nodes N_i and N_{i+1} prior to time t. Clearly if N_i has executed k times but N_{i+1} has not yet fired, then the number of tokens on Q_i is $k \cdot p_i$. It is also the case that after N_{i+1} executes for the first time, Q_i will always contain at least $\tau_i - c_i$ tokens. Sanjoy Baruah has observed that this *lower* bound on the minimum number of tokens on Q_i is not tight. Consider, for example, Q_i with $p_i = 8,\ \tau_i = 7,\ c_i = 6$. In this case, $\tau_i - c_i = 1$, but there will always be at least two tokens in the queue. The crucial observation made by Baruah is that the number of tokens in the queue, n, is always of the form $n = k_i \cdot p_i - k_{i+1} \cdot c_i$, where k_i and k_{i+1} represent the number of times N_i and N_{i+1} have executed respectively. We use this observation in Lemma 5.1 to bound the minimum number of tokens on Q_i after the first execution of N_{i+1} and the maximum number of tokens that can be on Q_i without the queue being over threshold.

Lemma 5.1. *The minimum possible number of tokens on Q_i after node N_{i+1} has fired once is m_i where*

$$m_i = \left\lceil \frac{\tau_i}{\gcd(p_i, c_i)} \right\rceil \cdot \gcd(p_i, c_i) - c_i \tag{5.1}$$

tokens, and the most tokens Q_i can hold without being over threshold is r_i where

$$r_i = \begin{cases} \tau_i - \gcd(p_i, c_i) & \text{if } \exists k : \tau_i = k \cdot \gcd(p_i, c_i) \\ \left\lfloor \frac{\tau_i}{\gcd(p_i, c_i)} \right\rfloor \cdot \gcd(p_i, c_i) & \text{otherwise} \end{cases} \tag{5.2}$$

Proof: Starting with Sanjoy Baruah's observation that the number of tokens in the queue, n, is always of the form $n = k_i \cdot p_i - k_{i+1} \cdot c_i$, we note that n takes on all values of $k \cdot \gcd(p_i, c_i)$:

$$\begin{aligned} \exists a, b, k : \quad k_i \cdot p_i - k_{i+1} \cdot c_i &= k_i \cdot (a \cdot \gcd(p_i, c_i)) - k_{i+1} \cdot (b \cdot \gcd(p_i, c_i)) \\ &= (k_i \cdot a - k_{i+1} \cdot b) \cdot \gcd(p_i, c_i) \\ &= k \cdot \gcd(p_i, c_i) \end{aligned}$$

To prove (5.1), we must find the smallest k such that $k \cdot \gcd(p_i, c_i) \geq \tau_i$ and then subtract c_i from this value since N_{i+1} consumes c_i tokens whenever it executes. Observe that the smallest k such that $k \cdot \gcd(p_i, c_i) \geq \tau_i$ is $k = \left\lceil \frac{\tau_i}{\gcd(p_i, c_i)} \right\rceil$. Therefore, the minimum number of tokens that will ever be on Q_i after N_{i+1} has executed at least once is:

$$m_i = \left\lceil \frac{\tau_i}{\gcd(p_i, c_i)} \right\rceil \cdot \gcd(p_i, c_i) - c_i = (5.1)$$

The most tokens Q_i can hold without being over threshold is $k' \cdot \gcd(p_i, c_i)$ where k' is the largest k such that $k \cdot \gcd(p_i, c_i) < \tau_i$. Observer that the largest k such that $k \cdot \gcd(p_i, c_i) \leq \tau_i$ is $k' = \left\lfloor \frac{\tau_i}{\gcd(p_i, c_i)} \right\rfloor$. Hence, if $\left\lfloor \frac{\tau_i}{\gcd(p_i, c_i)} \right\rfloor \cdot \gcd(p_i, c_i) < \tau_i$, (5.2) holds. But, if $k' \cdot \gcd(p_i, c_i) = \left\lfloor \frac{\tau_i}{\gcd(p_i, c_i)} \right\rfloor \cdot \gcd(p_i, c_i) = \tau_i$, then N_{i+1} is eligible for execution and Q_i is considered over threshold by Definition 5.1. In this case, the most tokens Q_i can hold without being over threshold is $(k' - 1) \cdot \gcd(p_i, c_i) = \tau_i - \gcd(p_i, c_i)$, and (5.2) holds for this case as well. □

Example 5.2. Applying Lemma 5.1 to the queue labeled Q_i in $Chain_3$ of Figure 4, we find

$$m_i = \left\lceil \frac{\tau_i}{\gcd(p_i, c_i)} \right\rceil \cdot \gcd(p_i, c_i) - c_i = \left\lceil \frac{7}{\gcd(4, 3)} \right\rceil \cdot \gcd(4, 3) - 3 = \left(\left\lceil \frac{7}{1} \right\rceil \cdot 1 \right) - 3 = 4$$

and $r_i = \tau_i - \gcd(p_i, c_i) = 7 - 1 = 6$.

Unlike Q_i in $Chain_3$, none of produce and consume values for the queues of the SAR graph are relatively prime. In fact, except for the queues labeled *RCS* and *Azimuth*, all of the queues have equal produce, threshold, and consume values. For these queues $m_i = r_i = 0$. For the queue labeled *Azimuth*, $\tau_i = c_i = \gcd(p_i, c_i) = 128$; hence, $m_i = r_i = 0$. The queue labeled *RCS* provides a more interesting example. In this case, $p_i = 256$, $\tau_i = 256 \cdot 128$, and $c_i = 256 \cdot 64$. Applying Lemma 5.1 to this queue yields:

$$\begin{aligned} m_i &= \left\lceil \frac{256 \cdot 128}{\gcd(256, 256 \cdot 64)} \right\rceil \cdot \gcd(256, 256 \cdot 64) - (256 \cdot 64) \\ &= \left(\left\lceil \frac{256 \cdot 128}{256} \right\rceil \cdot 256 \right) - (256 \cdot 64) \\ &= (128 \cdot 256) - (256 \cdot 64) = 256 \cdot 64 \end{aligned}$$

and $r_i = \tau_i - \gcd(p_i, c_i) = (256 \cdot 128) - 256 = 256 \cdot 127$. We will use these r_i values in §7 to bound the memory needs of the SAR graph. □

The following lemma, which will be used to prove Lemma 5.3 in §5.2, establishes the relationship for the number of executions of N_{i+1} as a function of the number of tokens produced by N_i.

Lemma 5.2. *Given $l \geq \tau_i$ tokens on Q_i, N_{i+1} will execute $\left\lfloor \frac{r-\tau_i}{c_i} \right\rfloor + 1$ times, consume $\left(\left\lfloor \frac{l-\tau_i}{c_i} \right\rfloor + 1\right) \cdot c_i$ tokens, and leave l' tokens on Q_i where $\left\lceil \frac{\tau_i}{\gcd(p_i,c_i)} \right\rceil \cdot \gcd(p_i, c_i) - c_i \ \leq \ l' \ < \ \tau_i$.*

Proof:[2] The number of times N_{i+1} will execute is the least natural number n such that $l - (n \cdot c_i) < \tau_i$, which implies $n > (l - \tau_i)/c_i$. The smallest natural number satisfying this inequality is $\left\lfloor \frac{l-\tau_i}{c_i} \right\rfloor + 1$. Since each execution of N_{i+1} consumes c_i tokens from Q_i, it immediately follows that the number of tokens consumed is $\left(\left\lfloor \frac{l-\tau_i}{c_i} \right\rfloor + 1\right) \cdot c_i$. By Lemma 5.1, $m_i = \left\lceil \frac{\tau_i}{\gcd(p_i,c_i)} \right\rceil \cdot \gcd(p_i, c_i) - c_i \leq l' \leq r_i < \tau_i$. Therefore, $\left\lceil \frac{\tau_i}{\gcd(p_i,c_i)} \right\rceil \cdot \gcd(p_i, c_i) - c_i \ \leq \ l' \ < \ \tau_i$, and the lemma holds. □

Lemma 5.2 establishes the execution relationship that exists between producer/consumer nodes, but it does not tell us the frequency with which the node will execute — only how many times the consumer will execute given some number of tokens generated by the producer. The rate at which nodes execute is the subject of the next section.

5.2 Node Execution Rates

PGM does not explicitly define temporal properties for the graph. However, the execution rate of every node in a graph is defined by the graph topology, the definition of nodes, the dataflow attributes, and the rate at which the source node produces data. Thus, given only the rate at which a source node delivers data, the execution rates of all other nodes can be derived. This fundamental property of real-time dataflow is the basis of the results presented in this section.

Most real-time execution models define task execution to be *periodic* or *sporadic*. Each time a task is ready to execute, it is said to be *released*. A periodic task is released exactly once every p time units (and p is called the period of the task). At least p time units separate every release of a sporadic task — no upper bound is given on subsequent releases of a sporadic task. Even when the source node of a PGM chain is periodic, the execution of the other nodes in the graph cannot be described as either periodic or sporadic. For example, consider $Chain_3$ of Figure 4. If N_i executes at times 0, y, $2y$, ..., N_{i+1} is eligible for one execution at times y and $2y$, but twice at time $3y$. For this instance of the problem, we may be able to model N_{i+1} as two periodic or sporadic tasks (that interleave their execution), but this technique does not generalize. If the consume value is 5 rather than 3, we get a very different execution pattern. When the source is not periodic and data arrives in bursts, which is common in many implementations, even modeling a node as x invocations of a $(1, y)$ periodic or sporadic task is insufficient. An execution paradigm that supports generic rates of the form x executions in y time units is required to analyze the execution of generic dataflow graphs.

We assume the strong synchrony hypothesis of [5] to introduce the concept of node execution rates. Under the synchrony hypothesis, we assume the graph executes on an infinitely fast machine. Hence, each node takes

[2] We thank the anonymous reviewer of [7] who suggested this proof and the proof of Lemma 5.3.

"no time" to execute and data passes from source to sink node instantaneously. The synchrony hypothesis lets us define rate executions in the absence of scheduling algorithms and deadlines. Node execution rates are defined as follows.

Definition 5.6. The time of the j^{th} execution of node N_i is represented as $T_{i,j}$.

Definition 5.7. An execution rate is a pair (x, y). A node N_i, $\forall i > 0$, executes at rate $R_i = (x_i, y_i)$ if, $\forall j > 0$, N_i executes exactly x_i times in all time intervals of $[t + y_i \cdot (j-1), t + y_i \cdot j)$ where $t > T_{i,1}$.

Throughout this paper, we assume constant produce, threshold, and consume values with $c_i \leq \tau_i$. If the produce and consume values for a node are not constant, then the node's maximum produce and minimum consume values can be used to determine the maximum execution rate. We also assume a periodic source. As implied by Theorem 5.4, a periodic source is not required for our analysis techniques. All lemmas and theorems in this paper can be generalized to support the analysis of graphs that receive data from source nodes specified by rates rather than periods.

Given a periodic source node, N_0, we present and prove the execution rate for N_1, the second node in the chain. Theorem 5.4 is a generalization of Lemma 5.3.

Lemma 5.3. *Assuming the strong synchrony hypothesis and no tokens on Q_0 prior to the beginning of graph execution, if $R_0 = (1, \rho)$ is the execution rate of N_0 with $T_{0,1} = 0$, then $R_1 = (x_1, y_1)$ is the execution rate of N_1 where $x_1 = \frac{p_0}{\gcd(p_0, c_0)}$ and $y_1 = \frac{c_0}{\gcd(p_0, c_0)} \cdot \rho$.*

Proof: Let $t > T_{1,1}$, and l be the number of tokens on Q_0 before any executions of N_1 at time t. By Lemma 5.2, $\left\lceil \frac{\tau_0}{gcd(p_0, c_0)} \right\rceil \cdot gcd(p_0, c_0) - c_0 \leq \ l < \tau_0$. Since $R_0 = (1, \rho)$, a total of $p_0 \cdot \frac{c_0}{\gcd(p_0, c_0)}$ tokens are enqueued on Q_0 over the interval $[t, t + y_1)$. Since each execution of N_1 removes c_0 tokens, x_1 executions during the interval $[t, t + y_1)$ will leave $(l + p_0 \cdot \frac{c_0}{\gcd(p_0, c_0)}) - (c_0 \cdot \frac{p_0}{\gcd(p_0, c_0)}) = l$ tokens on Q_0. Furthermore, no more executions could have occurred since the ${x_1}^{th}$ execution leaves $l < \tau_0$ tokens on Q_0. Any fewer executions would have left $l > \tau_0$ tokens on Q_0, and another execution of N_1 would have occurred. Therefore, exactly x_{i+1} executions take place in this interval.

Simple induction shows that N_1 will execute exactly $\frac{p_0}{\gcd(p_0, c_0)}$ times in all intervals of

$$\left[t + (j-1) \cdot \frac{c_0}{\gcd(p_0, c_0)} \cdot \rho, \quad t + j \cdot \frac{c_0}{\gcd(p_0, c_0)} \cdot \rho \right), \ \forall j > 0$$

where $t > T_{1,1}$, leaving l tokens on Q_0 at the end of each interval. Therefore R_1 is a valid rate specification for N_1. □

Theorem 5.4. $\forall i \geq 0$*: Assuming the strong synchrony hypothesis and no tokens on Q_i prior to the beginning of graph execution, if $R_0 = (x_0, y_0)$ is the execution rate of N_0, then the execution rate of N_{i+1} is $R_{i+1} = (x_{i+1}, y_{i+1})$ where $x_{i+1} = \frac{p_i}{\gcd(p_i \cdot x_i, c_i)} \cdot x_i$ and $y_{i+1} = \frac{c_i}{\gcd(p_i \cdot x_i, c_i)} \cdot y_i$.*

Proof: (by induction on i) Let $i = 0$ be the base case, $t > T_{1,1}$, and l be the number of tokens on Q_0 before any executions of N_1 at time t. If $x_0 = 1$ then Theorem 5.4 holds by Lemma 5.3. If $x_0 > 1$ then a total

of $(p_0 \cdot x_0) \cdot \frac{c_0}{\gcd(p_0 \cdot x_0, c_0)}$ tokens are enqueued on Q_0 over the interval $[t, t + y_1)$. Since each execution of N_1 removes c_0 tokens, x_1 executions during the interval $[t, t + y_1)$ will leave

$$(l + (p_0 \cdot x_0) \cdot \frac{c_0}{\gcd(p_0 \cdot x_0, c_0)}) - (c_0 \cdot \frac{p_0}{\gcd(p_0 \cdot x_0, c_0)} \cdot x_0) = l$$

tokens on Q_0. The rest of the proof for $i = 0$ and $x_0 > 1$ follows the proof of Lemma 5.3. Therefore, Theorem 5.4 holds for $i = 0$.

Assume by the induction hypothesis that Theorem 5.4 holds $\forall i : 0 \leq i < n$. Let $i = n - 1$, and l_i be the number of tokens on Q_i before any executions of N_{i+1} at time $t' > T_{i+1,1}$. By the induction hypothesis, N_i executes x_i times in all intervals of $[t + y_i \cdot (j-1), t + y_i \cdot j)$ where $t > T_{i,1}$ and $j > 0$. Observe that $T_{i+1,1} \geq T_{i,1}$. Therefore R_i also holds $\forall t \geq t' > T_{i+1,1}$, and N_i executes $x_i \cdot \frac{c_i}{\gcd(p_i \cdot x_i, c_i)}$ times in the interval $[t', t' + \frac{c_i}{\gcd(p_i \cdot x_i, c_i)} \cdot y_i)$. Let $x_{i+1} = \frac{p_i}{\gcd(p_i \cdot x_i, c_i)} \cdot x_i$ and $y_{i+1} = \frac{c_i}{\gcd(p_i \cdot x_i, c_i)} \cdot y_i$. Then N_i enqueues a total of $p_i \cdot x_i \cdot \frac{c_i}{\gcd(p_i \cdot x_i, c_i)}$ tokens on Q_i over the interval $[t', t' + y_{i+1})$. Since each execution of N_{i+1} removes c_i tokens, x_{1+1} executions during the interval $[t', t' + y_{i+1})$ will leave

$$(l_i + (p_i \cdot x_i) \cdot \frac{c_i}{\gcd(p_i \cdot x_i, c_i)}) - (c_i \cdot \frac{p_i}{\gcd(p_i \cdot x_i, c_i)} \cdot x_i) = l_i$$

tokens on Q_i.

Simple induction shows that N_{i+1} will execute exactly x_{i+1} times in all intervals of

$$[t' + (j-1) \cdot y_{i+1}, \quad t' + j \cdot y_{i+1}), \ \forall j > 0$$

where $t' > T_{i+1,1}$, leaving l_i tokens on Q_i at the end of each interval. Therefore, Theorem 5.4 holds for all $\forall i : 0 \leq i \leq n$. □

Example 5.3. We now apply Theorem 5.4 to the SAR graph shown in Figure 1 on page 4 to derive the execution rate of each node in the graph (excluding the *Sink* node, which represents an external device). We will use these numbers later to illustrate latency and buffer bounds.

Assume the *Source* node delivers one pulse (i.e., 118 tokens) every 3.6 *ms* and let $y = 3.6$, which means the source has an execution rate of $R_0 = (1, 3.6) = (1, y)$. The execution rate of the other nodes (excluding the *Sink* node) is derived as follows:

$$\begin{aligned} R_{Zero\ Fill} = (x_1, y_1) &= \left(\frac{p_0 \cdot x_0}{\gcd(p_0 \cdot x_0, c_0)}, \frac{c_0 \cdot y_0}{\gcd(p_0 \cdot x_0, c_0)} \right) \\ &= \left(\frac{p_{Range} \cdot x_0}{\gcd(p_{Range} \cdot x_0, c_{Range})}, \frac{c_{Range} \cdot y_0}{\gcd(p_{Range} \cdot x_0, c_{Range})} \right) \\ &= \left(\frac{118 \cdot 1}{\gcd(118 \cdot 1, 118)}, \frac{118 \cdot y}{\gcd(118 \cdot 1, 118)} \right) = \left(\frac{118}{118}, \frac{118y}{118} \right) = (1, y) \quad \Rightarrow \quad \begin{cases} x_1 = 1 \\ y_1 = y \end{cases} \end{aligned}$$

$$\begin{aligned} R_{Window\ Data} &= \left(\frac{p_1 \cdot x_1}{\gcd(p_1 \cdot x_1, c_1)}, \frac{c_1 \cdot y_1}{\gcd(p_1 \cdot x_1, c_1)} \right) = \left(\frac{p_{Fill} \cdot 1}{\gcd(p_{Fill} \cdot 1, c_{Fill})}, \frac{c_{Fill} \cdot y}{\gcd(p_{Fill} \cdot 1, c_{Fill})} \right) \\ &= \left(\frac{256 \cdot 1}{\gcd(256 \cdot 1, 256)}, \frac{256 \cdot y}{\gcd(256 \cdot 1, 256)} \right) = \left(\frac{256}{256}, \frac{256y}{256} \right) = (1, y) \quad \Rightarrow \quad \begin{cases} x_2 = 1 \\ y_2 = y \end{cases} \end{aligned}$$

$$R_{Range\ FFT} = R_{RCS\ Mult} = \left(\frac{256}{256}, \frac{256y}{256}\right) = (1, y)$$

$$R_{Corner\ Turn} = \left(\frac{256 \cdot 1}{\gcd(256 \cdot 1, 256 \cdot 64)}, \frac{(256 \cdot 64) \cdot y}{\gcd(256 \cdot 1, 256 \cdot 64)}\right) = \left(\frac{256}{256}, \frac{(256 \cdot 64)y}{256}\right) = (1, 64y)$$

$$R_{Azimuth\ FFT} = \left(\frac{(256 \cdot 128) \cdot 1}{\gcd((256 \cdot 128) \cdot 1, 128)}, \frac{128 \cdot 64y}{\gcd((256 \cdot 128) \cdot 1, 128)}\right) = \left(\frac{256 \cdot 128}{128}, \frac{128 \cdot 64y}{128}\right) = (256, 64y)$$

$$R_{Kernel\ Mult} = R_{Azimuth\ IFFT} = \left(\frac{128 \cdot 256}{\gcd(128 \cdot 256, 128)}, \frac{128 \cdot 64y}{\gcd(128 \cdot 256, 128)}\right) = (256, 64y) = (256, 230.4ms)$$

□

The first three nodes have execution rates of $(1, 3.6\ ms)$. That is, they execute once every 3.6 *ms*. The *Corner Turn* node executes once every 230.4 *ms* and the last four nodes execute 256 times every 230.4 *ms*.

5.3 RBE Task Model

Moving from the strong synchrony hypothesis to an actual implementation, we need to implement the graph as one or more tasks. A scheduling algorithm and a schedulability test that will analytically determine whether or not a graph will meet its temporal requirements are also necessary. We have already seen that nodes are neither periodic nor sporadic, even when the source is periodic, which eliminates most execution models from the literature. Nevertheless, it is appealing to implement each node as a task that is released when the input queue goes over threshold. If we schedule the tasks using the preemptive *earliest deadline first* (EDF) scheduling algorithm [13], we can verify the real-time requirements of the application using the techniques Jeffay has developed for the *Rate Based Execution* (RBE) model [10].

RBE is a general task model that consists of a collection of independent processes specified by four parameters: (x, y, d, e). The pair (x, y) represents the execution rate of a RBE task where x is the number of executions expected in an interval of length y. The response time parameter d specifies the maximum time between release of the task and the completion of its execution (i.e., d is the relative deadline). The parameter e is the maximum amount of processor time required for one execution of the task.

A RBE task set is feasible if there exists a preemptive schedule such that the j^{th} release of task T_i at time $t_{i,j}$ is guaranteed to complete execution by time $D_i(j)$, where

$$D_i(j) = \begin{cases} t_{i,j} + d_i & \text{if } 1 \leq j \leq x_i \\ \max(t_{i,j} + d_i, D_i(j - x_i) + y_i) & \text{if } j > x_i \end{cases} \tag{5.3}$$

The RBE task model makes no assumptions regarding when a task will be released, but the second line of the deadline assignment function (5.3) ensures that no more than x_i deadlines come due in an interval of length y_i, even when more than x_i releases of T_i occur in an interval of length y_i.

We use the following lemma, which bounds the processor demand in an interval, to prove the RBE feasibility condition of Theorem 5.6.

Lemma 5.5. *For preemptive scheduling of the execution of a task* $T = (x, y, d, e)$,

$$\forall L > 0, \quad f\left(\frac{L-d+y}{y}\right) \cdot x \cdot e \tag{5.4}$$

is a least upper bound on the number of units of processor time required to be available in the interval $[0, L]$ *to ensure that no job of* T *misses a deadline in* $[0, L]$, *where*

$$f(a) = \begin{cases} \lfloor a \rfloor & \text{if } a \geq 0 \\ 0 & \text{if } a < 0 \end{cases}$$

Proof: Define the processor demand of a task in an interval $[a, b]$ as the amount of processor time required to be available in $[a, b]$ to ensure that no release of T misses a deadline in $[a, b]$. To derive a least upper bound on the amount of processor time required to be available in the interval $[0, L]$, it suffices to consider a set of release times of T that results in the maximum processor demand in $[0, L]$. If t_j is the time of the j^{th} release of task T, then clearly the set of release times $t_j = 0$, $\forall j > 0$, is one such set. Under these release times, $\forall k \geq 0$, x releases of T have deadlines in the intervals $[k \cdot y, (k+1)y]$.

More precisely, x releases of T have deadlines in $[0, d]$. After d time units have elapsed, x releases of T have deadlines every y time units, and thus the number of releases with deadlines in the interval $[d, L]$ is $f\left(\frac{L-d}{y}\right) \cdot x$. Therefore, $\forall L \geq d$, the number of releases of T with deadlines in the interval $[0, L]$ is

$$x + f\left(\frac{L-d}{y}\right) \cdot x = \left(1 + f\left(\frac{L-d}{y}\right)\right) \cdot x = f\left(\frac{L-d}{y} + 1\right) \cdot x = f\left(\frac{L-d+y}{y}\right) \cdot x. \tag{5.5}$$

$\forall L < d$, no releases of T have deadlines in $[0, L]$, hence the right hand side of (5.5) gives the maximum number of releases of T with deadlines in the interval $[0, L]$, $\forall L > 0$.

Finally, as each release of T requires e units of processor time to execute to completion, (5.4) is a least upper bound on the number of units of processor time required to be available in the interval $[0, L]$ to ensure that no release of T misses a deadline in $[0, L]$. □

Note that there are many sets of task release times that maximize the processor demand of a task in the interval $[0, L]$. For example, given the recurrence relation for deadlines (5.3), it is straightforward to show that the less pathological set of task release times $t_j = \left\lfloor \frac{j-1}{x} \right\rfloor \cdot y$, $\forall j > 0$, also maximizes the processor demand of task T in the interval $[0, L]$.

Theorem 5.6. *Let* $\mathcal{T} = \{(x_1, y_1, d_1, e_1), \ldots (x_n, y_n, d_n, e_n)\}$ *be a set of RBE tasks.* $\mathcal{T}$ *will be feasible if and only if*

$$\forall L > 0, \quad L \geq \sum_{i=1}^{n} f\left(\frac{L-d_i+y_i}{y_i}\right) \cdot x_i \cdot e_i \tag{5.6}$$

$$\text{where } f(a) = \begin{cases} \lfloor a \rfloor & \text{if } a \geq 0 \\ 0 & \text{if } a < 0 \end{cases}$$

Proof: ($\Rightarrow$) We show the necessity of (5.6) by establishing the contrapositive, i.e., $\neg$(5.6) implies that $\mathcal{T}$ is not feasible. To show that $\mathcal{T}$ is not feasible it suffices to demonstrate the existence of a set of job release times t_{ij} for which at least one release of a task in $\mathcal{T}$ misses a deadline.

Assume $\neg(5.6)$, that is,

$$\exists L > 0 : L < \sum_{i=1}^{n} f\left(\frac{L - d_i + y_i}{y_i}\right) \cdot x_i \cdot e_i.$$

Consider the set of release times $t_{ij} = 0$, $\forall i : 1 \leq i \leq n$, and $\forall j > 0$, where t_{ij} is the time of the j^{th} release of task T_i. By Lemma 5.5, $\forall i$, task T_i requires $f\left(\frac{L-d_i+y_i}{y_i}\right) \cdot x_i \cdot e_i$ units of processor time in the interval of $[0, L]$. Therefore, for $\mathcal{T}$ to be feasible, we require that $\sum_{i=1}^{n} f\left(\frac{L-d_i+y_i}{y_i}\right) \cdot x_i \cdot e_i$ units of work be available in $[0, L]$. However, since

$$L < \sum_{i=1}^{n} f\left(\frac{L - d_i + y_i}{y_i}\right) \cdot x_i \cdot e_i,$$

a release of a task in $\mathcal{T}$ must miss a deadline in $[0, L]$. Thus there exist a set of release times such that a deadline is missed when $\neg(5.6)$. This proves the contrapositive.

($\Leftarrow$) To show the sufficiency of (5.6) we show that the preemptive EDF scheduling algorithm can schedule all releases of tasks in $\mathcal{T}$ without any job missing a deadline if the tasks satisfy (5.6). This is shown by contradiction.

Assume that $\mathcal{T}$ satisfies (5.6) and yet there exists a release of a task in $\mathcal{T}$ that misses a deadline at some point in time when $\mathcal{T}$ is scheduled by the EDF algorithm. Let t_d be the earliest point in time at which a deadline is missed and let t_o bet the later of:

- the end of the last interval prior to t_d in which the processor has been idle (or 0 if the processor has never been idle), or
- the latest time prior to t_d at which a task's release with deadline after t_d stops executing prior to t_d (or time 0 if such a release does not execute prior to t_d).

By the choice of t_o, (1) only releases with deadlines less than or equal to time t_d execute in the interval $[t_o, t_d]$, and (2) the processor is fully used in $[t_o, t_d]$. At most $\sum_{i=1}^{n} f\left(\frac{t_d - t_o - d_i + y_i}{y_i}\right)$ releases of tasks in $\mathcal{T}$ satisfy the conditions in (1), thus, if the EDF scheduling algorithm is used, $\sum_{i=1}^{n} f\left(\frac{L-d_i+y_i}{y_i}\right) \cdot x_i \cdot e_i$ is the least upper bound on the units of processor time required to be available in the interval $[t_o, t_d]$ to ensure that no task release misses a deadline in $[t_o, t_d]$. Let $\mathcal{E}$ be the amount of processor time consumed by tasks in $\mathcal{T}$ in the interval $[t_o, t_d]$ when scheduled by the EDF algorithm. It follows that

$$\sum_{i=1}^{n} f\left(\frac{L - d_i + y_i}{y_i}\right) \cdot x_i \cdot e_i \geq \mathcal{E}.$$

Since the processor is fully used in the interval $[t_o, t_d]$, and since a deadline is missed at time t_d, it follows that $\mathcal{E}$ is greater than the processor time available in the interval $[t_o, t_d]$, namely $t_d - t_o$. Hence,

$$\sum_{i=1}^{n} f\left(\frac{L - d_i + y_i}{y_i}\right) \cdot x_i \cdot e_i \geq \mathcal{E} > t_d - t_o.$$

However this contradicts our assumption that $\mathcal{T}$ satisfies (5.6). Hence if $\mathcal{T}$ satisfies (5.6), then no release of a task in $\mathcal{T}$ misses a deadline when $\mathcal{T}$ is scheduling by the EDF algorithm. It follows that satisfying (5.6) is a sufficient condition for feasibility. □

Note that if the cumulative processor utilization for a graph is strictly less than one (i.e., $\sum_{i=1}^{n} \frac{x_i \cdot e_i}{y_i} < 1$) then condition (5.6) can be evaluated efficiently (in pseudo-polynomial time) using techniques developed in [2] and applied in [3] and [11].

For a PGM graph, (5.6) becomes a sufficient condition (but not necessary) for preemptive EDF scheduling as long as nodes execute only when their input queues are over threshold (i.e., the tasks are released when the node's input queue is over threshold — thereby ensuring precedence constraints are met). (5.6) is not a necessary condition for PGM graphs since it assumes that all x_i releases of a node may occur at the beginning of an interval of length y_i. For some nodes, such as N_{i+1} in Figure 4 on page 7, this is not possible.

6 Latency

We now address the issue of latency, and begin by defining latency in the context of signal processing graphs. We then demonstrate, using the strong synchrony hypothesis, that there exist multiple latency values for a graph and show how these latency values relate to latency induced by the scheduling algorithm. Finally, we analyze the affect of deadlines on latency.

6.1 What is Latency?

Latency can be defined many different ways. An appealing definition is the delay between a start event and a corresponding stop event. In graph models that require unity dataflow attributes, the start event may be the arrival of a token from the source and the stop event can be identified as the enqueuing of a token on the graph's output queue. But it is difficult to apply this definition to PGM graphs. As the SAR graph demonstrates, nodes may add tokens to the data stream. Nodes may also reduce the number of tokens in the data stream (known as data decimation), or the node may delay some number of tokens and use the delayed tokens in both the current and the subsequent execution as the *Corner Turn* node does in the SAR graph.

A signal processing engineer describes latency as the time delay between the sampling of a signal and the presentation of the processed signal to the output device (which may be a screen, speaker, or another computer). We use this definition with a clarification. Since we can only measure time in units of the period of the source, we consider the p_0 tokens delivered each period by N_0 to be "one sample"; each pulse in the SAR graph constitutes one sample, which consists of 118 tokens. Hence, under the strong synchrony hypothesis, latency is the delay between the enqueuing of p_0 tokens onto Q_0 by the source node N_0 and the next enqueuing of p_n tokens on Q_n by node N_n.

Latency is a function of the scheduling algorithm. It is the case for graph models, however, that latency also has a structural component. The next section illustrates this property.

6.2 Latency with the Strong Synchrony Hypothesis

There is a pattern of executions that result in various latency values for the input signal. Consider the execution of the SAR graph shown in Figure 5. In this example, we assume the strong synchrony hypothesis

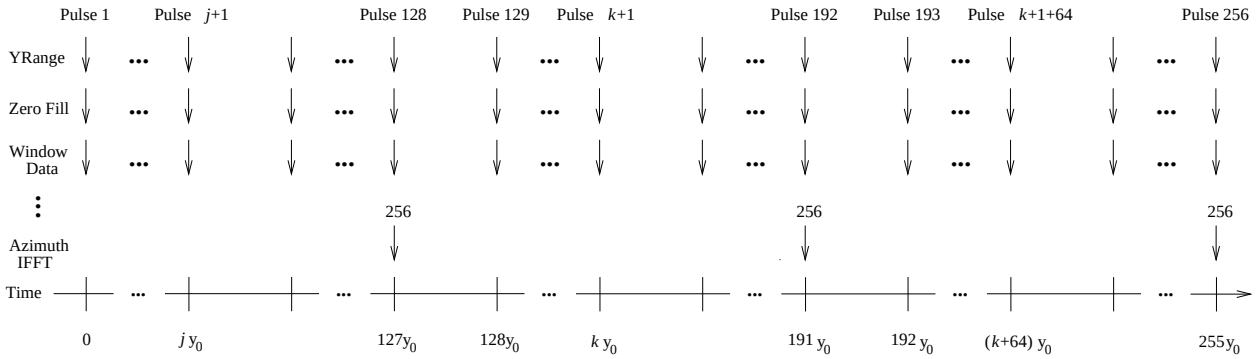


Figure 5: Latency for the SAR graph under strong synchrony hypothesis. Each down arrow represents the release and instantaneous execution of a node.

and each down arrow represents the release and instantaneous execution of a node. The minimum latency for a sample is zero, which is the case for the 128^{th} pulse received by the SAR graph. As shown in Figure 5, the 128^{th} pulse arrives at time $127y_0$ and results in the execution of every node in the graph. Pulses 192, 256, 320, 384, ... all have a latency of 0. The maximum latency value, encountered by the first pulse, is $127y_0$. The first signal received by the graph always encounters the maximum latency (assuming the queues have no initial data). There is, however, another "maximum" latency that is of more interest, and that is the maximum latency that occurs after the first execution of every node in the graph. In the execution example shown in Figure 5 for the SAR graph, this maximum latency is encountered by pulses 129, 193, 257, 321, ..., which have a latency of $63y_0$. Notice that there are 126 other unique latency values for this simple graph (e.g., the latency for pulse j+1 is $(127-j)y_0$).

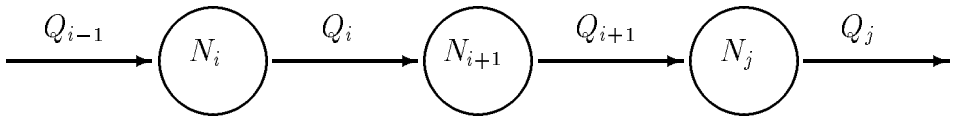
The latency encountered by a sample of the signal (under the strong synchrony hypothesis) is dependent on the data flow attributes of the graph and the state of the queues (i.e., the number of tokens on each queue of the graph) when the sample arrives. We can determine the magnitude of a sample's latency by determining how many more samples are required before node N_n executes. Lemma 6.1 fulfills this role.

Lemma 6.1. *Given $l_k < \tau_k$ tokens on Q_k $\forall k : i \leq k < j$, N_i must execute $F(N_i, N_j)$ times to produce enough data to put Q_{j-1} over threshold (and thus making N_j eligible for execution) where*

$$\forall i,j : 0 \leq i < j \leq n :: F(N_i,N_j) = \begin{cases} \left\lceil \frac{\tau_i - l_i}{p_i} \right\rceil & \text{if } i+1 = j \\ \left\lceil \frac{(F(N_{i+1},N_j)-1)\cdot c_i + \tau_i - l_i}{p_i} \right\rceil & \text{if } i+1 < j \end{cases} \tag{6.1}$$

Proof: **Case 1:** $i+1=j$. If there are l_i tokens on Q_i and $l_i < \tau_i$, then $\tau_i - l_i$ more tokens are required before N_j is eligible for execution. Since N_i produces p_i tokens every time it executes, it follows that N_i must execute $\left\lceil \frac{\tau_{j-1} - l_{i-1}}{p_{j-1}} \right\rceil$ times before N_j is eligible for execution, and (6.1) holds for $i+1=j$.

Case 2: $i+1<j$ (by induction on i). We work the induction backward by starting with the maximum i that satisfies $i+1<j$ and decreasing i to 0. For the base case, let $i=j-2$ ($\Rightarrow i+1=j-1$):



As in the previous case, N_{i+1} must execute $x = \left\lceil \frac{\tau_{i+1} - l_{i+1}}{p_{i+1}} \right\rceil$ times before N_j is eligible for execution. Therefore, we need only answer how many times N_i must execute for N_{i+1} to execute x more times. From **Case 1**, we know that $\tau_i - l_i$ more tokens are needed for N_{i+1} to execute once. Since N_{i+1} consumes c_i tokens every time it executes, the remaining $x - 1$ executions require an additional $(x-1) \cdot c_i$ tokens to be produced by N_i. Hence, N_i must execute

$$\left\lceil \frac{(x-1) \cdot c_i + \tau_i - l_i}{p_i} \right\rceil = \left\lceil \frac{\left(\left\lceil \frac{\tau_{i+1} - l_{i+1}}{p_{i+1}} \right\rceil - 1 \right) \cdot c_i + \tau_i - l_i}{p_i} \right\rceil = \left\lceil \frac{(F(N_{i+1}, N_j) - 1) \cdot c_i + \tau_i - l_i}{p_i} \right\rceil \qquad (6.2)$$

times before N_j is eligible to execute again, and (6.1) holds for $i = j - 2$.

Assume, by the induction hypothesis, that (6.1) holds $\forall i, j : 0 < i < j \leq n$. Let $i = 0$. By the induction hypothesis, N_1 must execute $F(N_1, N_j)$ times before N_j is eligible for execution. Therefore, we need only answer how many times N_0 must execute for N_1 to execute $F(N_1, N_j)$ times. Applying (6.2) from the base case, with $i = 0$ and $x = F(N_1, N_j)$, N_0 must execute

$$\left\lceil \frac{(F(N_1, N_j) - 1) \cdot c_0 + \tau_0 - l_0}{p_0} \right\rceil = F(N_0, N_j)$$

times and (6.1) holds. Therefore (6.1) holds $\forall i, j : 0 \leq i < j \leq n$. □

Evaluating $F(N_0, N_n)$ just before the i^{th} sample's arrival will tell us how many samples are required before N_n will be eligible for execution. Hence, as implied by Lemma 6.2, the latency the i^{th} sample will encounter is given by $(F(N_0, N_n) - 1) \cdot y_0$ when $F(N_0, N_n)$ is evaluated just before the sample arrives. We subtract one from $F(N_0, N_n)$ before converting it to time units since the latency interval begins after the sample arrives.

Lemma 6.2. *Given $R_0 = (1, \rho)$. When $F(N_0, N_n)$ is evaluated just before the sample's arrival,*

$$\textit{Sample Latency} = (F(N_0, N_n) - 1) \cdot \rho \qquad (6.3)$$

Proof: By Lemma 6.1, N_0 must execute $F(N_0, N_n) - 1$ more times after the signal arrives if $F(N_0, N_n)$ is evaluated just before the signal arrives. Therefore, under the strong synchrony hypothesis, if N_0 has a period of ρ, the sample's latency will be $(F(N_0, N_n) - 1) \cdot \rho$. □

Using Lemma 6.2 we find, as expected, that the latency of the first pulse received by the SAR graph is $127y_0$. Recall from Lemma 5.1 that the most tokens Q_i can hold without being over threshold is r_i and the minimum possible number of tokens on Q_i after node N_{i+1} has fired once is m_i. When all of the queues in the graph contain r_i tokens, as is the case just before pulses 192, 256, 320, ..., the next sample's latency will be 0 — just as Figure 5 shows. Evaluating (6.3) when each queue in the SAR graph contains m_i tokens, we get a sample latency of $64y_0$ — just as Figure 5 shows for pulses 129 and 193.

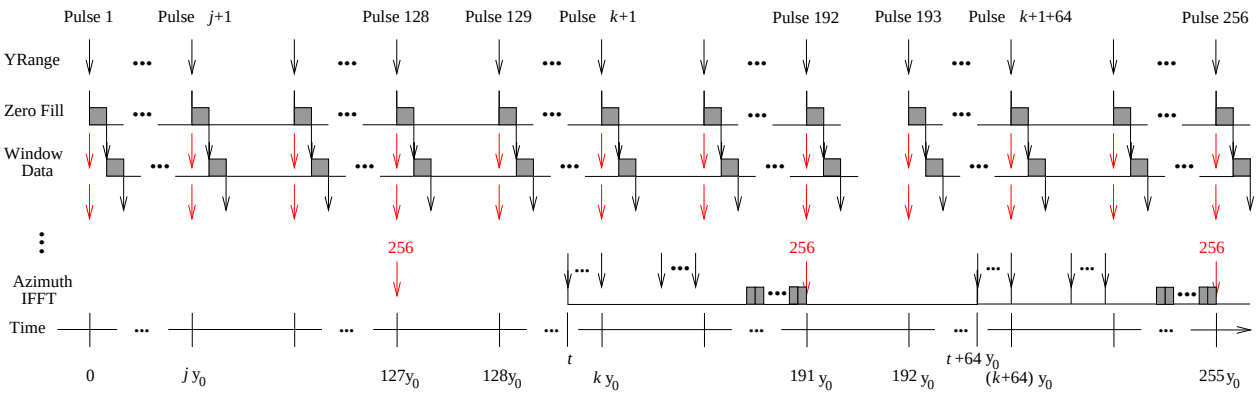


Figure 6: Latency for the SAR graph. A light arrow represents a node's release under the strong synchrony hypothesis. A dark arrow represents the actual release time, and the node's execution is represented by a box.

6.3 Latency in an Implementation

Scheduling an implementation of the graph results in an upper and lower bound for each of the latency values identified with the strong synchrony hypothesis. In other words, we get latency intervals rather than precise latency values for a given sample.

The lower bound for a sample's latency is a function of the scheduling algorithm and, as shown in §6.2, the graph attributes. The lower bound for the latency interval is the latency value derived using (6.3) plus the sum of the execution times for the nodes in the chain. That is, a sample's latency must be greater than or equal to $(F(N_0, N_n) - 1) \cdot y_0 + \sum_{i=1}^{n} e_i$.

The upper bound for a sample's latency is dependent on the scheduling algorithm, dataflow attributes, and deadline values. Generally, the deadline parameters are the only free variables in the function. To determine a sample's latency in an implementation of the graph, we need to provide a value for each d_i in the RBE task set. Realizing that d_i affects latency, what should it be? How does d_i affect latency?

We start by observing that if, $\forall i : 1 \leq i \leq n$, $d_i = y_i$ and the graph is not schedulable (i.e., (5.6) returns a negative result) then the processor is overloaded since (5.6) reduces to the Lui & Layland feasibility test [13] and we get $1 < \sum_{i=1}^{n} \frac{x_i \cdot e_i}{y_i}$. We also observe that increasing $d_i > y_i$ will not improve latency and, as we will show later, increases buffer requirements. Hence, we will set $d_i = y_i$ and see how this affects the upper bound for latency values.

Figure 6 shows an execution of the SAR graph with $d_i = y_i$. In this figure, the light arrows represent the release time for N_i under the strong synchrony hypothesis and the dark arrows represent the actual release time. We see from Figure 6 that task *Zero Fill* is released at times 0, y_0, $2y_0$, $3y_0$, ..., and the deadlines corresponding to each release time is y_0, $2y_0$, $3y_0$, ... since $d_1 = y_1 = y_0$. Due to scheduling and execution times, however, the task *Window Data* is not released until times $0 + e_1$, $y_0 + e_1$, $2y_0 + e_1$, $3y_0 + e_1$, ..., and the corresponding deadlines are $0 + e_1 + d_2 = y_0 + e_1$, $2y_0 + e_1$, $3y_0 + e_1$, ... In this example, the first execution of task *Azimuth IFFT* is released at time t, which is after $128y_0$. Its deadline is $t + 64y_0$, which is after $192y_0$. Also note that the 256^{th} execution of task *Azimuth IFFT* completes execution by time $191y_0$

— well before its deadline.

The release times shown in Figure 6 for the tasks *Zero Fill* and *Window Data* are the earliest possible release times. As we have noted, the task *Azimuth IFFT* completes its 256^{th} execution by time $191y_0$ even though the deadline for the first release of *Azimuth IFFT* is not until $t + 64y_0$. This was no accident. All of the first 256 executions of *Azimuth IFFT* will be released and complete execution between $127y_0$ and $191y_0$. To see this, we must look at the earliest possible release time for the first execution of *Azimuth IFFT* and the schedulability condition (5.6). From Lemma 6.2, we know that the first release of task *Azimuth IFFT* cannot occur before $127y_0$. An affirmative result from (5.6) means that there exists enough processor capacity for nodes N_1 thru N_k, $1 \leq i \leq k \leq n$, to execute $\frac{y_k}{y_i} \cdot x_i$ times during an interval of length y_k. This means that 64 executions of *Zero Fill*, *Window Data*, *Range FFT*, and *RCS Mult*; 1 execution of *Corner Turn*; and 256 executions of *Azimuth FFT*, *Kernel Mult*, and *Azimuth IFFT* will all complete execution within $64y_0$ time units even when they are all released at the same instant (i.e., when *Zero Fill* is first released). We will exploit this fact, similarly to the way Jeffay did in [9], to bound a sample's latency.

We can use the release point derived with the strong synchrony hypothesis and add d_i to get the time at which N_i will have completed execution — even if this time is less than the actual release time plus d_i. Theorem 6.3 uses this fact to provide a lower and upper bound for any sample's latency.

Theorem 6.3. *Given $R_0 = (1, \rho)$ and a schedulable graph in which $\forall i : 1 \leq 1 < n :: d_i \leq d_{i+1}$, a sample's latency under EDF scheduling with deadline assignment function* (5.3) *is bounded such that*

$$(F(N_0, N_n) - 1) \cdot \rho + \sum_{i=1}^{n} e_i \quad \leq \quad \textit{Sample Latency} \quad \leq \quad (F(N_0, N_n) - 1) \cdot \rho + d_n$$

where $F(N_0, N_n)$ is evaluated just before the sample's arrival.

Proof: By Lemma 6.2, a sample's latency in an implementation of the graph cannot be less than $(F(N_0, N_n) - 1) \cdot \rho)$ since this is the latency on a infinitely fast machine. The minimum latency for a signal occurs when each node in the chain must only execute once after N_0 delivers the additional $(F(N_0, N_n) - 1) \cdot p_0$ tokens. Therefore the sample's latency must be greater than or equal to $(F(N_0, N_n) - 1) \cdot \rho + \sum_{i=1}^{n} e_i$. Let $sample_k$ be the sample for which we are bounding latency. When the $(F(N_0, N_n) - 1)^{th}$ sample after $sample_k$ arrives, every node in the graph will fire at least once before N_n produces data. Using deadline inheritance, every task released (either directly or indirectly) from this last sample will have a deadline less than or equal to d_n time units from the arrival of the last signal. Therefore if the graph is schedulable, N_n will execute within $(F(N_0, N_n) - 1) \cdot \rho + d_n$ time units of the arrival of $sample_k$. Hence, a sample's latency is bounded such that

$$(F(N_0, N_n) - 1) \cdot \rho + \sum_{i=1}^{n} e_i \leq \text{ Sample Latency } \leq (F(N_0, N_n) - 1) \cdot \rho + d_n$$

where $F(N_0, N_n)$ is evaluated just before the sample's arrival and Theorem 6.3 holds. □

Theorem 6.3 tells us that if a graph is schedulable by (5.6), task N_i will complete execution within d_i time units of the release time calculated under the strong synchrony hypothesis. Therefore, if we let the

released task N_i *inherit* the release time of its predecessor in the dataflow graph (i.e., N_{i-1}) and calculate its deadline by adding d_i to this *logical* release time, we get a deadline equal to the time that Theorem 6.3 states the task will have finished executing. Since the first node of a chain receives data from an external device, it has no release time to inherit and its logical release time is the same as its actual release time. Consider the execution diagram of Figure 6. Node *Zero Fill* is first released at time 0. The first actual release of *Window Data* occurs after *Zero Fill* completes execution, at time e_1, and its deadline is set to $y_0 + e_1$. The logical release of *Window Data*, however, occurs at time 0 since this is the release time inherited from *Zero Data*. (It is also the release time derived under the strong synchrony hypothesis.) Using the logical release time, we get a deadline of y_0 for *Zero Data*, which is the time Theorem 6.3 gave as the upper bound for when the task will finish execution if the task set is schedulable. Similarly, we get a logical release time of $127y_0$ and a deadline of $191y_0$ for the first execution of *Azimuth IFFT*.

As long as the scheduler ensures that a task only executes when its input queue is over threshold, it does not matter if N_{i+1} executes before N_i. When the RBE task set is specified such that $d_i \leq d_{i+1}$, a release of N_{i+1} will never be assigned a deadline earlier than a release of N_i, even when logical release times are used. Moreover, the latency bound of Theorem 6.3 holds even when a release of N_{i+1} executes before a release of N_i, which may occur when both are assigned the same deadline. The EDF scheduling algorithm does not specify how to break ties. Hence, a variant of EDF may break ties based on topological sorting rather than actual release times, which may result in N_{i+1} executing before N_i when $d_i = d_{i+1}$. Although latency is not affected by the tie breaking algorithm, buffer bounds are. We address this issue in §7.

6.4 Reducing Latency Further

If the latency bounds derived using $d_i = y_i$ do not meet the application's latency requirements, we can evaluate the latency with smaller deadlines. As long as we keep $d_i \leq d_{i+1}$, Theorem 6.3 can be used to evaluate new latency bounds. A simple technique to reduce the maximum latency any signal will encounter (for a graph executing on a uniprocessor) is to iteratively decrease the maximum deadline(s) to the maximum y_i such that $y_i < \max\{d_j\}$ in the graph. For example, after a positive result from (5.6) with $d_n = y_n$, we would set $d_n = y_{n-1}$, assuming $y_{n-1} < y_n$, otherwise we would set $d_{n-1} = d_n = y_{n-2}$. When (5.6) finally returns a negative result we have found a "breaking point". We can either use the deadlines from the previous iteration or find *the* "breaking point" (for this technique), which lies between the deadline values used in the last two iterations.

7 Bounding Buffers

This sections gives bounds for the buffer requirements of chains executed under the RBE model with release inheritance, as described in the previous section. We use logical release times rather than actual release times so that deadline ties are created during execution. These ties can then be broken based on topology to reduce the buffer requirements from what they would be if the ties were broken arbitrarily.

Since N_{n+1} represents an external device and is not scheduled, we cannot give an upper bound on Q_n.

One may assume the device takes data as it is produced and bound the buffer space for Q_n with p_n. Or assuming double buffering techniques (common in I/O interfaces), one might bound the buffer space as $2p_n$. In either case, the bound is platform specific.

Recall from Lemma 5.1 that the most tokens Q_i can hold without being over threshold is r_i. After Q_i goes over threshold, the number of tokens that can accumulate on the queue is a function of dataflow attributes, deadlines, and the scheduling algorithm.

We have derived buffer bounds for preemptive EDF scheduling and two variations of EDF: Breadth-First EDF (BF-EDF) and Depth-First EDF (DF-EDF). The names for these EDF variants become apparent when one looks at a possible scheduling graph, which is used to break deadline ties. A scheduling graph is a topologically sorted graph of vertices representing releases of RBE tasks with the same deadline. The graph is sorted with respect to the dataflow graph and all jobs in the graph have the same deadline. Consider the scheduling graph in Figure 7 — a possible snapshot of the ready queue for the SAR graph after Pulse 128

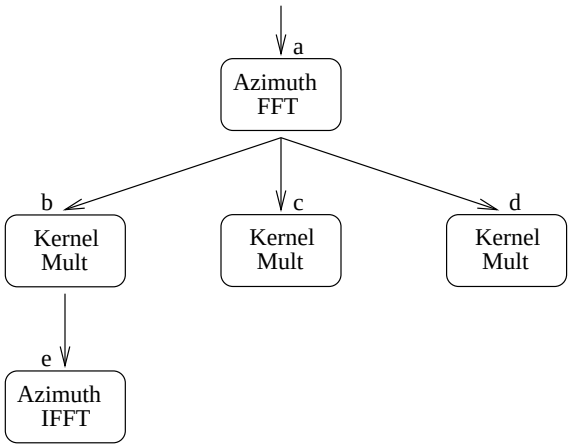


Figure 7: A scheduling graph.

has been processed by the *Corner Turn* node. The BF-EDF scheduling algorithm performs a breadth-first search of eligible jobs, beginning at the left most side of each level. Hence, the BF-EDF algorithm would select the *Azimuth FFT* task followed by the left most release of *Kernel Mult.* Using the labels *a, b, c, d,* and *e* to refer to the tasks releases in Figure 7, BF-EDF would schedule them in order: *a, b, c, d, d′, e* and e^* where d' represents the new release of *Kernel Mult* caused by the execution of *Azimuth FFT* and e^* represents the new releases of *Azimuth IFFT*, which result from executions of *Kernel Mult.* The DF-EDF scheduling algorithm performs a depth-first search of eligible jobs by traversing down the left most side of the tree until it reaches a leaf. In this case, DF-EDF would select the *Azimuth IFFT* task to execute followed by the left most release of *Kernel Mult.* A DF-EDF schedule, starting with the schedule graph of Figure 7, would be *e, b,* e'*, c,* e''*, d,* e'''*, a* where e', e'', and e''' are new releases of *Azimuth IFFT* caused by the executions of *Kernel Mult.*

7.1 Buffer Bounds for EDF Scheduling

We begin the process of bounding the buffer requirements of a graph by observing that when $d_{i+1} > d_i$, the buffer bound for Q_i is the same for all EDF variant scheduling algorithms that use release time inheritance to schedule PGM graphs. The case of $d_{i+1} > d_i$ prevents deadline ties from occurring; hence, the tie breaking algorithm has no impact on the buffer bound for Q_i. When $d_{i+1} > d_i$ and $d_{i+1} \geq y_0$, we can bound the buffer requirements of Q_i independent of the number of tokens that may accumulate on Q_{i-1}.

Lemma 7.1. *For EDF scheduling algorithms with release time inheritance, if $R_0 = (1, \rho)$ and $d_{j+1} > d_j \ \wedge \ d_{j+1} \geq y_0$, the maximum buffer space required by Q_i of a schedulable graph is less than or equal to*

$$B_{EDF}(Q_i) = \begin{cases} (\lceil \frac{d_1}{y_0} \rceil \cdot p_0) + r_0 & \text{if } i = 0 \\ (\lceil \frac{d_{i+1}}{y_i} \rceil \cdot x_i \cdot p_i) + r_i & \text{if } (i > 0 \ \wedge \ ((d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i) \ \vee \ (d_i < y_i \leq d_{i+1})) \\ (\lfloor \frac{d_{i+1}}{y_i} \rfloor \cdot x_i \cdot p_i) + r_i & \text{if } (i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}) \end{cases} \tag{7.1}$$

Proof: The proof proceeds by cases.

Case $i = 0$: The bound for Q_0 is independent of the tie breaking algorithm since N_0 is not scheduled; it adds p_0 tokens to Q_0 at times $0, y_0, 2y_0, 3y_0, \ldots$ independent of the scheduling algorithm. Therefore, when N_1 is released at time ky_0 (for some non-negative integer k), it will will be assigned a deadline of $ky_0 + d_1$.

If $d_1 \leq y_0$, then all executions of N_1 released prior to ky_0 will have completed execution by time ky_0 and the release of N_1 at ky_0 will complete by $ky_0 + d_1$. Therefore, the maximum number of tokens that can be on Q_i at any time is $p_0 + r_0 = (\lceil \frac{d_1}{y_0} \rceil \cdot p_0) + r_0$ and Lemma 7.1 holds for $i = 0$ and $d_1 \leq y_0$. Consider the case in which $d_1 > y_0$. During any interval of length d_1, N_0 can produce at most $(\lceil \frac{d_1}{y_0} \rceil \cdot p_0)$ tokens. If the interval begins with r_0 tokens on Q_0 then Lemma 7.1 holds.

What if the interval begins with τ_0 or more tokens on Q_0? Let $k'y_0$ be the last time Q_i went over threshold such that just before the produce of N_0 at time $k'y_0$, Q_0 held less then τ_0 tokens. Pick a time ky_0 such that $k'y_0 < ky_0 < k'y_0 + d_1$. At most $(\lceil \frac{d_1}{y_0} \rceil \cdot p_0)$ tokens will be produced during the interval $[k'y_0, \ k'y_0 + d_1)$. After the $\lceil \frac{p_0}{c_o} \rceil$ releases of N_1 with deadline $k'y_0 + d_1$ complete execution, Q_i will contain at most

$$\left(\left\lceil \frac{d_1}{y_0} \right\rceil \cdot p_0 + r_0 \right) - \left(\left\lceil \frac{p_0}{c_0} \right\rceil \cdot c_0 \right)$$

tokens. During every y_0 time units between $k'y_0 + d_1$ and $ky_0 + d_1$, between $\lfloor \frac{p_0}{c_0} \rfloor$ and $\lceil \frac{p_0}{c_0} \rceil$ deadlines for N_0 will come due and the number of tokens on Q_1 can never become greater than the bound for the interval of $[k'y_0, \ k'y_0 + d1)$, which is $(\lceil \frac{d_1}{y_0} \rceil \cdot p_0 + r_0)$ tokens in this case. Therefore, Lemma 7.1 holds for $i = 0$.

Case $i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i$: Observe $d_{i+1} < y_i \Rightarrow \left\lceil \frac{d_{i+1}}{y_i} \right\rceil = 1$. Let ky_0 be the release time of the first execution of N_i that will put Q_i over threshold. With release time inheritance, the deadline of N_{i+1} is $ky_0 + d_{i+1}$ and $ky_0 + d_i < ky_0 + d_{i+1} < ky_0 + y_i$. At most x_i releases of N_i will be assigned deadlines between ky_0 and $ky_0 + y_i$. Therefore, Q_i will contain no more than $x_i \cdot p_i + r_i$ tokens during this interval. Pick ky_0 such that the number of tokens on Q_i is greater than τ_i, then following the proof for the case of $i = 0$, we see that Q_i is still bounded from above by $\left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ and (7.1) holds for $i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i$.

Case $i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}$**:** Let ky_0 be the release time of the first execution of N_i that will put Q_i over threshold. With release time inheritance, the deadline of N_{i+1} is $ky_0 + d_{i+1}$ and $ky_0 + d_i < ky_0 + y_i \leq ky_0 + d_{i+1}$. At most x_i releases of N_i will be assigned deadlines between ky_0 and $ky_0 + y_i$. If $d_{i+1} = y_i$, then $d_i < y_i = d_{i+1}$ and Q_i will never contain more than $x_i \cdot p_i + r_i = \left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ tokens during this interval.

If $d_{i+1} > y_i$, then $d_i < y_i < d_{i+1}$. Any releases of N_i that occur at time $ky_0 + y_i$ will be assigned deadlines of $ky_0 + y_i + d_i$ and it may be the case (depending on the actual values of d_i, y_i, and d_{i+1}) that $ky_0 + y_i + d_i \leq ky_0 + d_{i+1}$. If $d_i < y_i < d_{i+1} < 2y_i$ then at most $\lceil \frac{d_{i+1}}{y_i} \rceil \cdot x_i \cdot p_i = 2x_i \cdot p_i$ tokens will be added to the queue during the interval $[ky_0, \ ky_0 + d_{i+1})$. Simple induction shows that (7.1) holds for all values of d_{i+1} such that, for some $j > 1$, $d_i < y_i \leq d_{i+1} < jy_i$ when the interval begins with at most r_i tokens. Pick ky_0 such that the number of tokens on Q_i is greater than r_i, then following the proof of the same case for $i = 0$, we see that Q_i is still bounded from above by $\left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ and (7.1) holds for $i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}$.

Case $i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}$**:** Let ky_0 be the release time of the first execution of N_i that will put Q_i over threshold. With release time inheritance, the deadline of N_{i+1} is $ky_0 + d_{i+1}$ and $ky_0 + y_i \leq ky_0 + d_i < ky_0 + d_{i+1}$. Let d_i and d_{i+1} be defined such that $y_i \leq d_i < d_{i+1} < 2y_i$. At most x_i releases of N_i will be assigned deadlines during ky_0 and $ky_0 + y_i$, and any more releases of N_i before $ky_0 + y_i$ will not have deadlines before $ky_0 + 2y_i$. Therefore, at most x_i deadlines of N_i will elapse between ky_0 and $ky_0 + d_{i+1}$. If $d_{i+1} = 2y_i$, $2x_i$ executions of N_i will complete before $ky_0 + d_{i+1}$, the deadline for N_{i+1}. Simple induction on the magnitude of d_{i+1} shows that (7.1) continues to bound the buffer requirements of Q_i. If the number of tokens on Q_i is greater than r_i at release time ky_0, then following the proof of the same case for $i = 0$, we see that Q_i is still bounded from above by $\left\lfloor \frac{d_{i+1}}{y_i} \right\rfloor \cdot x_i \cdot p_i + r_i$ and (7.1) holds for $i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}$. □

The EDF scheduling algorithm does not specify how deadline ties are broken, and the buffer requirements of a queue are greatest when breadth-first scheduling is used to break deadline ties between two eligible nodes. Thus, to bound a queue's buffer requirements, we must assume that whenever a deadline tie is possible it may be broken by performing a breadth-first search of the scheduling graph.

Lemma 7.2. *For EDF scheduling algorithms with release time inheritance that may break ties using a breadth-first search of the scheduling graph, if* $R_0 = (1, \rho)$*, the maximum buffer space required by* Q_i*,* $\forall i \geq 0$*, of a schedulable graph is less than or equal to*

$$B_{BF}(Q_i) = \begin{cases} (\lceil \frac{d_1}{y_0} \rceil \cdot p_0) + r_0 & \text{if } i = 0 \\ (\lceil \frac{d_{i+1}}{y_i} \rceil \cdot x_i \cdot p_i) + r_i & \text{if } (i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i) \\ & \quad \vee \ (i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}) \\ (\lfloor \frac{d_{i+1}}{y_i} \rfloor \cdot x_i \cdot p_i) + r_i & \text{if } (i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}) \\ \left(\left\lfloor \frac{B_{BF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right) \cdot p_i + r_i & \text{otherwise (i.e., } i > 0 \ \wedge \ (d_{i+1} = d_i \ \vee \ d_i < d_{i+1} < y_0)) \end{cases} \tag{7.2}$$

Proof: The proof proceeds by cases.

Case $i = 0$: By Lemma 7.1, the upper bound for Q_0 is $(\lceil \frac{d_1}{y_0} \rceil \cdot p_0 + r_0)$ tokens in this case. Therefore, (7.2) holds for $i = 0$.

Case $i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i$: By Lemma 7.1, Q_i is bounded from above by $\left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ and (7.2) holds for $i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i$.

Case $i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}$: By Lemma 7.1, Q_i is bounded from above by $\left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ and (7.2) holds for $i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}$.

Case $i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}$: By Lemma 7.1, Q_i is bounded from above by $\left\lfloor \frac{d_{i+1}}{y_i} \right\rfloor \cdot x_i \cdot p_i + r_i$ and (7.2) holds for $i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}$.

Case $i > 0 \ \wedge \ (d_{i+1} = d_i \ \vee \ d_i < d_{i+1} < y_0)$: (by induction on i) Let $i = 1$ and ky_0 be the release time of the first execution of N_1 that will put Q_1 over threshold. If $d_i < d_{i+1} < y_0$, then all eligible releases of N_1 and N_2 will complete execution before $(k+1)y_0$. Under EDF scheduling, all eligible executions of N_1 will complete before any eligible executions of N_2. Therefore the maximum number of tokens that will be on Q_1 is based on the number of times N_1 executes in $[ky_0, \ (k+1)y_0)$, which is based on the maximum size of Q_0 in the same interval. From the proof for the case of $i = 0$, we know that Q_0 will never contain more than $B_{BF}(Q_0)$ tokens. From Lemma 5.2 we know that given $B_{BF}(Q_0) \geq \tau_0$ tokens on Q_0, N_1 will execute $\left(\left\lfloor \frac{B_{BF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right)$ times. Therefore, Q_1 will contain at most $\left(\left\lfloor \frac{B_{BF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right) \cdot p_i + r_i$ tokens and (7.2) holds for $i = 1$ and $d_i < d_{i+1} < y_0$.

If $d_{i+1} = d_i$, then all releases of N_1 at time ky_0 will have the same deadline as any releases of N_2 caused by the execution of N_1 in the interval $[ky_0, \ ky_0 + d_1)$. Moreover, the next possible deadline for N_1 or N_2 is $(k+1)y_0$. Observe that the maximum number of tokens will accumulate on Q_1 when all released executions of N_1 complete before any released executions of N_2. Such is the case when a breadth-first search of the scheduling graph is used to break deadline ties. Therefore if deadline ties are broken using a breadth-first search of the scheduling graph, the maximum number of tokens Q_1 can have is determined by the maximum number of executions of N_1 that can be released at ky_0. From the previous paragraph, we know that this is $\left(\left\lfloor \frac{B_{BF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right)$. Therefore, Q_1 will contain at most $\left(\left\lfloor \frac{B_{BF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right) \cdot p_i + r_i$ tokens and (7.2) holds for $i = 1$ and $d_i = d_{i+1}$.

By the induction hypothesis on i, assume (7.2) holds for $\forall i : 1 \leq i < n-1$. Let $i = n-1$ and $d_i = d_{i+1}$ (i.e., $d_{n-1} = d_n$). The proof that (7.2) holds for $i = n-1$ and $d_i = d_{i+1}$ follows the same proof used for $i = 1$ and we see that (7.2) holds for all i such that $0 \leq i < n$. □

Since EDF does not specify how ties are broken, we need to sum $B_{BF}(Q_i)$ over all of the queues in the chain to bound a graph's simultaneous buffer requirements.

Theorem 7.3. *For EDF scheduling with release time inheritance, if $R_0 = (1, \rho)$ and $d_{i+1} \geq d_i$, $\forall i : 0 \leq i < n$, the maximum buffer space required is less than or equal to $\sum_{i=0}^{n-1} B_{BF}(Q_i)$.*

Proof: From Lemma 7.2, the maximum space Q_i will require is $B_{BF}(Q_i)$. Since EDF does not specify how ties are broken, we need to sum $B_{BF}(Q_i)$ over all of the queues in the chain to bound a graph's simultaneous buffer requirements. Therefore, the maximum buffer space required is less than or equal to $\sum_{i=0}^{n-1} B_{BF}(Q_i)$. □

If deadline ties are broken in a deterministic manner specified by the deadline driven scheduling algorithm, we can get a much tighter bound on buffer requirements.

7.2 Buffer Bounds for BF-EDF Scheduling

The BF-EDF scheduling algorithm is an EDF algorithm in which deadline ties are broken by performing a breadth-first search of the scheduling graph. The function $B_{BF}(Q_i)$, (7.2), returns the maximum number of tokens the i^{th} queue will ever hold when deadline ties *may* be broken with a breadth-first search of the scheduling graph. The BF-EDF algorithm *always* breaks ties with a breadth-first search of the scheduling graph, so we can use $B_{BF}(Q_i)$ to bound the memory needs of Q_i when a schedulable graph is executed under BF-EDF scheduling. When $d_i < d_{i+1}$, $\forall i > 0$, no deadline tie is possible and Theorem 7.3 bounds the graphs buffer requirements for BF-EDF scheduling as well as EDF scheduling. When there exists consecutive nodes in the chain with the same deadline, however, we can reduce the buffer bounds for the graph.

Consider the case when $d_i = d_{i+1}$, $\forall i > 0$. Since EDF does not specify how ties are broken, we had to sum $B_{BF}(Q_i)$ over all of the queues in the chain to bound a graph's simultaneous buffer requirements. With BF-EDF, however, we know that, $\forall j > i > 1$, any release of N_i will execute before a release of N_j when N_i and N_j both have the same deadline. When N_i executes, it reads data from Q_{i-1} and writes data to Q_i — using both queues simultaneously. By the time N_{i+1} executes, however, Q_{i-i} will be under threshold and will hold at most r_{i-1} tokens. Much of the space that was used by Q_{i-1} when N_i was executing can be reclaimed and used by Q_{i+1} to hold the data produced by N_{i+1}. Therefore the total buffer space required for Q_{i-1} and Q_{i+1} is

$$\max\{B_{BF}(Q_{i-1}) - r_{i-1}, B_{BF}(Q_{i+1}) - r_{i+1}\} + r_{i-1} + r_{i+1}.$$

Theorem 7.4 divides the queues into two disjoint sets and uses this technique to bound the total buffer space required by the chain when all of the nodes have the same deadline values.

Theorem 7.4. *For the BF-EDF scheduling algorithm with release time inheritance, if* $R_0 = (1, \rho)$ *and* $d_{i+1} = d_i$, $\forall i : 0 < i < n$, *the maximum buffer space required is* $\leq \beta$, *where*

$$\begin{aligned}\beta = B_{BF}(Q_0) &+ \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < n\} \\ &+ \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < n\} + \sum_{i=1}^{n-1} r_i\end{aligned} \tag{7.3}$$

Proof: Let the last queue in the chain be labeled Q_n. Then the chain has $n+1$ queues and $n+2$ nodes. The proof proceeds by case for $n = 0 \ldots 3$, and by induction on n for $n > 3$.

Case 1: $n = 0 \implies$ one queue and two nodes. The theorem holds vacuously for $n = 0$.

Case 2: $n = 1 \implies$ two queues and three nodes as in the graph of Figure 8.

Since N_2 represents an external device, we do not bound the space for Q_1 and the total buffer space

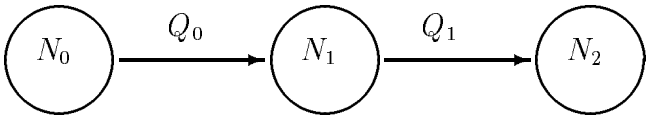


Figure 8: $n = 1 \implies$ 3 node chain

required by the 2 queue (3 node) chain is β where

$$\begin{aligned}\beta &\leq B_{BF}(Q_0) \\ &= B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < 1\} \\ &\quad + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i - 1 : i > 0 \ \wedge \ k < 1\} + \sum_{i=1}^{0} r_i\end{aligned}$$

and (7.3) holds for $n = 1$.

Case 3: $n = 2 \implies$ three queues and four nodes as in the graph of Figure 9.

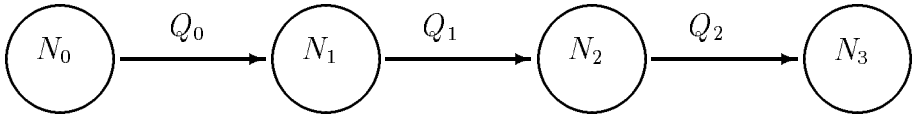


Figure 9: $n = 2 \implies$ 4 node chain

Since N_3 represents an external device, we do not bound the space for Q_2 and the total buffer space required by the 3 queue (4 node) chain is β where

$$\begin{aligned}\beta &\leq B_{BF}(Q_0) + B_{BF}(Q_1) = B_{BF}(Q_0) + (B_{BF}(Q_1) - r_1) + r_1 \\ &= B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < 2\} \\ &\quad + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i - 1 : i > 0 \ \wedge \ k < 2\} + \sum_{i=1}^{1} r_i\end{aligned}$$

and (7.3) holds for $n = 2$.

Case 4: $n = 3 \implies$ four queues and five nodes as in the graph of Figure 10.

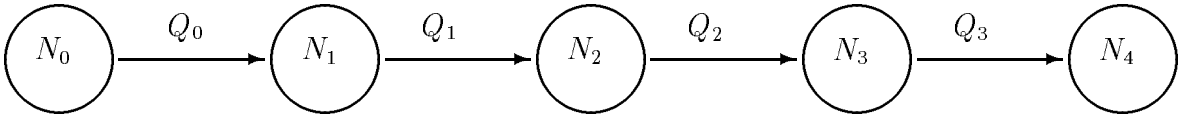


Figure 10: $n = 3 \implies$ 5 node chain

Since N_4 represents an external device, we do not bound the space for Q_3 and the total buffer space

required by the 4 queue (5 node) chain is β where

$$\begin{aligned}\beta &\leq B_{BF}(Q_0) + B_{BF}(Q_1) + B_{BF}(Q_2) = B_{BF}(Q_0) + (B_{BF}(Q_1) - r_1) + r_1 + (B_{BF}(Q_2) - r_2) + r_2 \\ &= B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < 3\} \\ &\quad + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < 3\} + \sum_{i=1}^{2} r_i\end{aligned}$$

and (7.3) holds for $n = 3$.

Case 5: by induction on n. Let $n = 4$ be the base case such that N_0 and N_{n+1} represent external devices as in the six node graph of Figure 11.

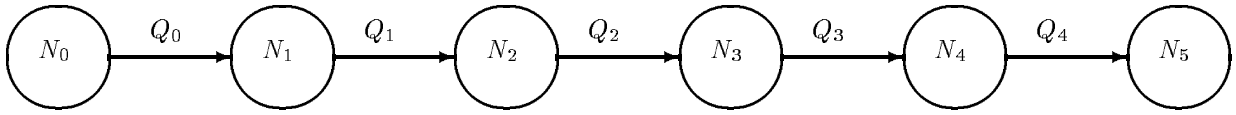


Figure 11: $n = 4 \implies$ 6 node chain

Theorem 7.4 does not bound the buffer space for Q_n so its space does not contribute to the total bound.

Since N_0 is not scheduled but N_1 is and $d_1 > y_0$ is allowed, $B_{BF}(Q_0)$ must be included in the upper bound. When N_1 executes it reads data from Q_0 and writes data to Q_1 — using both queues simultaneously. When N_2 executes it reads data from Q_1 and writes data to Q_2 and all three queues may be needed at the same time. When N_3 executes, however, Q_1 will be under threshold and will hold at most r_1 tokens. Much of the space that was used by Q_1 when N_2 was executing can be reclaimed and used by Q_3 to hold the data produced by N_3. Therefore, the total buffer space required for the 4 queues is β where

$$\begin{aligned}\beta &\leq B_{BF}(Q_0) + B_{BF}(Q_2) + \max\{B_{BF}(Q_1) - r_1, B_{BF}(Q_3) - r_3\} + r_1 + r_3 \\ &= B_{BF}(Q_0) + (B_{BF}(Q_2) - r_2) + \max\{B_{BF}(Q_1) - r_1, B_{BF}(Q_3) - r_3\} + r_1 + r_2 + r_3 \\ &= B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < 4\} \\ &\quad + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < 4\} + \sum_{i=1}^{3} r_i\end{aligned}$$

and (7.3) holds for $n = 4$. Assume by the induction hypothesis that (7.3) holds for $4 \leq n < N$. Let $n = N$. Recall we do not count the space for Q_n since N_{n+1} represents an external device and the bound on Q_n is platform specific.

Observe that when N_{n-1} executes under BF-EDF scheduling, $\forall k : 1 \leq k < (n-1)$, Q_k must be under threshold. If n is even,

$$\begin{aligned}\beta \leq \ & B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < n\} \\ & + \max\{B_{BF}(Q_{n-1}), \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < n-1\}\} + \sum_{i=1}^{n-1} r_i \\ = \ & B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i < 0 \ \wedge \ k < n\} \\ & + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < n\} + \sum_{i=1}^{n-1} r_i\end{aligned}$$

Similarly, if n is odd, the total buffer space for all queues must be less than or equal to β where

$$\begin{aligned}\beta &\leq B_{BF}(Q_0) + \max\{B_{BF}(Q_{n-1}), \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < n-1\}\} \\ &\quad + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < n\} + \sum_{i=1}^{n-1} r_i \\ &= B_{BF}(Q_0) + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < n\} \\ &\quad + \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i-1 : i > 0 \ \wedge \ k < n\} + \sum_{i=1}^{n-1} r_i\end{aligned}$$

In either case, (7.3) holds for $n = N$. Therefore by induction, Theorem 7.4 holds for $d_{i+1} = d_i, \ \forall i : 0 < i < n$.

□

Depending on the d_i values, we may be able to use variations of the techniques shown in this section to get tighter buffer bounds for a specific graph than either Theorem 7.3 or Theorem 7.4. We leave open the problem of finding a tight buffer bound for generic chains executed with the BF-EDF scheduling algorithm.

7.3 Buffer Bounds for DF-EDF Scheduling

The DF-EDF scheduling algorithm is an EDF algorithm in which deadline ties are broken by performing a depth-first search of the scheduling graph. For some applications, breaking deadline ties with a depth-first search of the scheduling graph rather than a breadth-first search results in a lower upper bound on buffer requirements for the graph. The function $B_{DF}(Q_i)$ returns the maximum number of tokens Q_i will ever hold when the graph is scheduled with release inheritance and DF-EDF. This function is used in Theorem 7.6 to bound the total buffer space required for the graph to execute with DF-EDF scheduling.

Lemma 7.5. *For the Depth-first EDF scheduling algorithm with release time inheritance, if the graph is schedulable, $R_0 = (1, \rho)$, and $d_{i+1} \geq d_i, \ \forall i : 0 \leq i < n$, the maximum buffer space required by Q_i is less than or equal to*

$$B_{DF}(Q_i) = \begin{cases} (\lceil \frac{d_1}{y_0} \rceil \cdot p_0) + r_0 & \text{if } i = 0 \\ (\lceil \frac{d_{i+1}}{y_i} \rceil \cdot x_i \cdot p_i) + r_i & \text{if } (i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i) \\ & \quad \vee \ (i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}) \\ (\lfloor \frac{d_{i+1}}{y_i} \rfloor \cdot x_i \cdot p_i) + r_i & \text{if } (i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}) \\ \left(\left\lfloor \frac{B_{BF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right) \cdot p_i + r_i & \text{if } i > 0 \ \wedge \ d_i < d_{i+1} < y_0 \\ p_i + r_i & \text{otherwise (i.e., } i > 0 \ \wedge \ d_{i+1} = d_i) \end{cases} \tag{7.4}$$

Proof: The proof proceeds by cases.

Case $i = 0$: By Lemma 7.1, the upper bound for Q_0 is $(\lceil \frac{d_1}{y_0} \rceil \cdot p_0 + r_0)$ tokens in this case. Therefore, (7.4) holds for $i = 0$.

Case $i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i$: By Lemma 7.1, Q_i is bounded from above by $\left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ and (7.4) holds for $i > 0 \ \wedge \ d_{i+1} > d_i \ \wedge \ y_0 \leq d_{i+1} < y_i$.

Case $i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}$: By Lemma 7.1, Q_i is bounded from above by $\left\lceil \frac{d_{i+1}}{y_i} \right\rceil \cdot x_i \cdot p_i + r_i$ and (7.4) holds for $i > 0 \ \wedge \ d_i < y_i \leq d_{i+1}$.

Case $i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}$**:** By Lemma 7.1, Q_i is bounded from above by $\left\lfloor \frac{d_{i+1}}{y_i} \right\rfloor \cdot x_i \cdot p_i + r_i$ and (7.4) holds for $i > 0 \ \wedge \ y_i \leq d_i < d_{i+1}$.

Case $i > 0 \ \wedge \ (d_{i+1} = d_i \ \vee \ d_i < d_{i+1} < y_0)$**:** (by induction on i)

Case $i > 0 \ \wedge \ d_i < d_{i+1} < y_0$**:** (by induction on i) Let $i = 1$ and ky_0 be the release time of the first execution of N_1 that will put Q_1 over threshold. If $d_i < d_{i+1} < y_0$ then all eligible releases of N_1 and N_2 will complete execution before $(k+1)y_0$. Therefore the maximum number of tokens that will be on Q_1 is based on the number of times N_1 executes in $[ky_0, \ (k+1)y_0)$, which is based on the maximum size of Q_0 in the same interval. From the proof for the case of $i = 0$, we know that Q_0 will never contain more than $B_{DF}(Q_0)$ tokens. From Lemma 5.2 we know that given $B_{DF}(Q_0) \geq \tau_0$ tokens on Q_0, N_1 will execute $\left(\left\lfloor \frac{B_{DF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right)$ times. Therefore, Q_1 will contain at most $\left(\left\lfloor \frac{B_{DF}(Q_{i-1}) - \tau_{i-1}}{c_{i-1}} \right\rfloor + 1 \right) \cdot p_i + r_i$ tokens and (7.1) holds for $i = 1$ and $d_i < d_{i+1} < y_0$.

By the induction hypothesis on i, assume (7.4) holds for $\forall i : 1 \leq i < n-1$. Let $i = n-1$ and $i > 0 \ \wedge \ d_i < d_{i+1} < y_0$. The proof that (7.4) holds for $i = n-1$ and $i > 0 \ \wedge \ d_i < d_{i+1} < y_0$ follows the same proof outlined above and we see that (7.4) holds for all i such that $0 \leq i < n$.

Case $i > 0 \ \wedge \ d_{i+1} = d_i$**:** (by induction on i) Let $i = 1$ and ky_0 be the release time of the first execution of N_1 that will put Q_1 over threshold. If $d_{i+1} = d_i$, then all releases of N_1 at time ky_0 will have the same deadline as any releases N_2 caused by the execution of N_1 in the interval $[ky_0, \ ky_0 + d_1)$. Moreover, the next possible deadline for N_1 or N_2 is $(k+1)y_0$. Since DF-EDF breaks deadline ties with a depth-first search of the scheduling graph, releases of N_2 with the same deadline of N_1 will execute before the release of N_1 and the maximum number of tokens Q_1 can have is $p_1 + r_1$. Therefore, (7.4) holds for $i = 1$ and $d_i = d_{i+1}$.

By the induction hypothesis on i, assume (7.4) holds for $\forall i : 1 \leq i < n-1$. Let $i = n-1$ and $d_i = d_{i+1}$ (i.e., $d_{n-1} = d_n$). The proof that (7.4) holds for $i = n-1$ and $d_i = d_{i+1}$ follows the same proof outlined above and we see that (7.4) holds for all i such that $0 \leq i < n$. □

Theorem 7.6. *For DF-EDF scheduling with release time inheritance, if* $R_0 = (1, \rho)$ *and* $d_{i+1} \geq d_i$, $\forall i : 0 < i < n$, *the maximum buffer space required is less than or equal to* $\sum_{k=0}^{n-1} B_{DF}(Q_k)$.

Proof: From Lemma 7.5, the maximum space Q_k will require is $B_{DF}(Q_k)$. Therefore, the maximum buffer space required is less than or equal to $\sum_{k=0}^{n-1} B_{DF}(Q_k)$. □

When the graph is scheduled with the BF-EDF algorithm and $d_{i+1} = d_i, \ \forall i : 0 < i < n$, Theorem 7.4 provides a tighter bound on the buffer space required by the graph than Theorem 7.3 by reclaiming unused buffer space. Unfortunately we cannot use the same technique when the graph is scheduled with the DF-EDF algorithm to get a tighter bound than Theorem 7.6 provides. To see this, consider the graph of Figure 12 and let $R_0 = (1, \rho)$. Under DF-EDF scheduling, every time N_4 executes, Q_3 will require space for 4 tokens. At the same time Q_1 will require space for 6 tokens (not $r_1 = 0$ as it does with BF-EDF scheduling).

We leave open the problem of finding a tight buffer bound for generic chains executed with the DF-EDF scheduling algorithm.

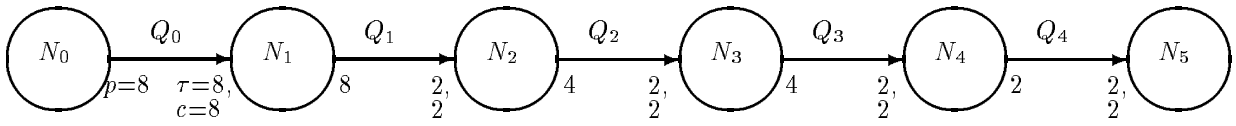


Figure 12: 6 node chain scheduled with the DF-EDF algorithm

7.4 Buffer Bounds for the SAR graph

This section develops buffer bounds for the SAR graph using different d_i values and scheduling algorithms by applying Theorems 7.3, 7.4, and 7.6. The SAR graph of Figure 1 is replicated below in Figure 13 to make it easier to follow the derivations.

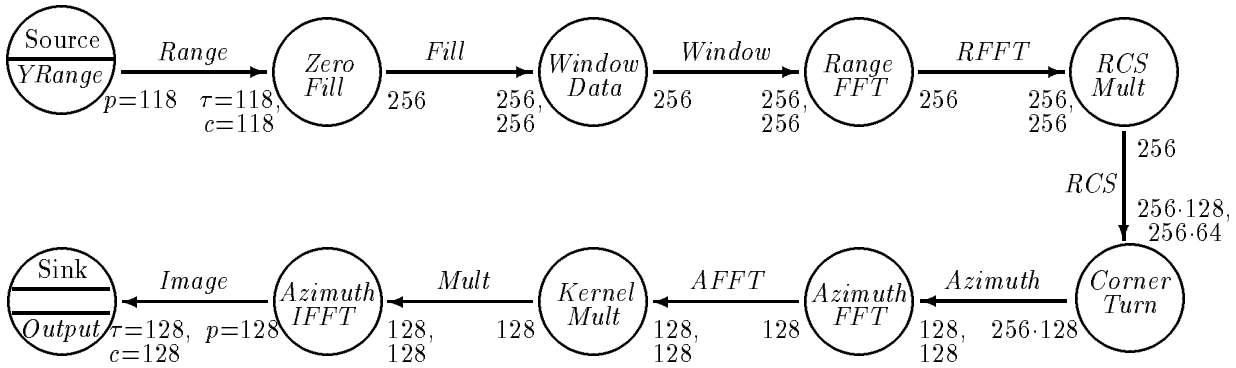


Figure 13: SAR Graph

We begin by finding the minimum buffer space required to execute the graph. This occurs when we set $d_i = y_0$, $\forall i > 0$, assuming we have a fast enough CPU that the graph is schedulable with these deadline values. Observe that $d_i = y_0$, $\forall i > 0$, also minimizes the latency any sample will encounter. Let $R_{YRange} = (1, 3.6ms)$, as in Example 5.3, and each $d_i = 3.6ms$. We will also use the r_i values derived in Example 5.2.

EDF and BF-EDF Scheduling with $\mathbf{d_i = y_0}$. To bound the graph's buffer needs when it is executed with either canonical EDF or BF-EDF scheduling, we first need to bound the buffer requirements of each queue using $B_{BF}(Q_i)$, (7.2):

$$\begin{aligned} B_{BF}(Q_0 = Range) &= \left(\left\lceil \frac{d_{Zero\ Fill}}{y_{YRange}} \right\rceil \cdot p_{Range} \right) + r_{Range} \\ &= \left(\left\lceil \frac{3.6ms}{3.6ms} \right\rceil \cdot 118 \right) + 0 = 118 \end{aligned}$$

$$\begin{aligned} B_{BF}(Q_1 = Fill) &= \left(\left\lfloor \frac{B_{BF}(Range) - \tau_{Range}}{c_{Range}} \right\rfloor + 1 \right) \cdot p_{Fill} + r_{Fill} \\ &= \left(\left\lfloor \frac{118 - 118}{118} \right\rfloor + 1 \right) \cdot 256 + 0 = (0 + 1) \cdot 256 = 256 \end{aligned}$$

$$
\begin{aligned}
B_{BF}(Q_2 = Window) &= \left(\left\lfloor \frac{B_{BF}(Fill) - \tau_{Fill}}{c_{Fill}} \right\rfloor + 1 \right) \cdot p_{Window} + r_{Window} \\
&= \left(\left\lfloor \frac{256 - 256}{256} \right\rfloor + 1 \right) \cdot 256 + 0 = (0 + 1) \cdot 256 = 256
\end{aligned}
$$

$$
\begin{aligned}
B_{BF}(Q_3 = RFFT) &= \left(\left\lfloor \frac{B_{BF}(Window) - \tau_{Window}}{c_{Window}} \right\rfloor + 1 \right) \cdot p_{RFFT} + r_{RFFT} \\
&= \left(\left\lfloor \frac{256 - 256}{256} \right\rfloor + 1 \right) \cdot 256 + 0 = (0 + 1) \cdot 256 = 256
\end{aligned}
$$

$$
\begin{aligned}
B_{BF}(Q_4 = RCS) &= \left(\left\lfloor \frac{B_{BF}(RFFT) - \tau_{RFFT}}{c_{RFFT}} \right\rfloor + 1 \right) \cdot p_{RCS} + r_{RCS} \\
&= \left(\left\lfloor \frac{256 - 256}{256} \right\rfloor + 1 \right) \cdot 256 + (256 \cdot 127) \\
&= 256 + (256 \cdot 127) = 256 \cdot 128 = 32768
\end{aligned}
$$

$$
\begin{aligned}
B_{BF}(Q_5 = Azimuth) &= \left(\left\lfloor \frac{B_{BF}(RCS) - \tau_{RCS}}{c_{RCS}} \right\rfloor + 1 \right) \cdot p_{Azimuth} + r_{Azimuth} \\
&= \left(\left\lfloor \frac{(256 \cdot 128) - (256 \cdot 128)}{256 \cdot 64} \right\rfloor + 1 \right) \cdot (256 \cdot 128) + 0 \\
&= 256 \cdot 128 = 32768
\end{aligned}
$$

$$
\begin{aligned}
B_{BF}(Q_6 = AFFT) &= \left(\left\lfloor \frac{B_{BF}(Azimuth) - \tau_{Azimuth}}{c_{Azimuth}} \right\rfloor + 1 \right) \cdot p_{AFFT} + r_{AFFT} \\
&= \left(\left\lfloor \frac{(256 \cdot 128) - 128}{128} \right\rfloor + 1 \right) \cdot 128 + 0 \\
&= (255 + 1) \cdot 128 = 256 \cdot 128 = 32768
\end{aligned}
$$

$$
\begin{aligned}
B_{BF}(Q_7 = Mult) &= \left(\left\lfloor \frac{B_{BF}(AFFT) - \tau_{AFFT}}{c_{AFFT}} \right\rfloor + 1 \right) \cdot p_{Mult} + r_{Mult} \\
&= \left(\left\lfloor \frac{(256 \cdot 128) - 128}{128} \right\rfloor + 1 \right) \cdot 128 + 0 \\
&= (255 + 1) \cdot 128 = 256 \cdot 128 = 32768
\end{aligned}
$$

These results are summarized in Table 1.

By Theorem 7.3, the total buffer space required to execute the SAR graph with EDF scheduling when $d_i = y_0 = 3.6ms$ is less than or equal to $\sum_{i=0}^{n-1} B_{BF}(Q_i) = 131,958$. By Theorem 7.4, if BF-EDF scheduling is used when $d_i = y_0 = 3.6ms$, the required buffer spaced is less than or equal to β where

$$
\begin{aligned}
\beta = B_{BF}(Q_0) &+ \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i : i > 0 \ \wedge \ k < n\} \\
&+ \max\{B_{BF}(Q_k) - r_k \mid \forall k = 2i - 1 : i > 0 \ \wedge \ k < n\} + \sum_{i=1}^{n-1} r_i \\
&= 118 + 32,768 + 32,768 + 32,512 = 98,116
\end{aligned}
$$

Queue	$B_{BF}(Q_i)$ $d_i = y_0$	$B_{DF}(Q_i)$ $d_i = y_0$	$B_{BF}(Q_i)$ $d_i = y_i$	$B_{DF}(Q_i)$ $d_i = y_i$
Range	118	118	118	118
Fill	256	256	256	256
Window	256	256	256	256
RFFT	256	256	256	256
RCS	32,768	32,768	48,896	48,896
Azimuth	32,768	32,768	32,768	32,768
AFFT	32,768	128	32,768	128
Mult	32,768	128	32,768	128

Table 1: Maximum buffer space required per queue evaluated with $B_{BF}(Q_i)$ and $B_{DF}(Q_i)$.

DF-EDF Scheduling with $\mathbf{d_i = y_0}$. To bound the graph's buffer needs when it is executed with DF-EDF scheduling, we first need to bound the buffer requirements of each queue using $B_{DF}(Q_i)$, (7.4):

$$\begin{aligned}
B_{DF}(Q_0 = Range) &= \left(\left\lceil \frac{d_{Zero\ Fill}}{y_{Y\,Range}} \right\rceil \cdot p_{Range} \right) + r_{Range} \\
&= \left(\left\lceil \frac{3.6ms}{3.6ms} \right\rceil \cdot 118 \right) + 0 = 118 \\
B_{DF}(Q_1 = Fill) &= p_{Fill} + r_{Fill} = 256 + 0 = 256 \\
B_{DF}(Q_2 = Window) &= p_{Window} + r_{Window} = 256 + 0 = 256 \\
B_{DF}(Q_3 = RFFT) &= p_{RFFT} + r_{RFFT} = 256 + 0 = 256 \\
B_{DF}(Q_4 = RCS) &= p_{RCS} + r_{RCS} = 256 + (256 \cdot 127) = 256 \cdot 128 = 32768 \\
B_{DF}(Q_5 = Azimuth) &= p_{Azimuth} + r_{Azimuth} = (256 \cdot 128) + 0 = 32768 \\
B_{DF}(Q_6 = AFFT) &= p_{AFFT} + r_{AFFT} = 128 + 0 = 128 \\
B_{DF}(Q_7 = Mult) &= p_{Mult} + r_{Mult} = 128 + 0 = 128
\end{aligned}$$

These results are summarized in Table 1.

By Theorem 7.6, the total buffer space required to execute the SAR graph with DF-EDF scheduling when $d_i = y_0 = 3.6ms$ is less than or equal to $\sum_{i=0}^{n-1} B_{DF}(Q_i) = 66,678$.

Scheduling with $\mathbf{d_i = y_i}$. Now consider what happens to the buffer bounds when $\forall i > 0 : d_i = y_i$. Table 1 shows the values returned from $B_{BF}(Q_i)$ and $B_{DF}(Q_i)$ for each queue in the SAR graph with $d_i = y_i$. Notice that only the queue labeled *RCS* is affected by the new deadline values. This is because the *Corner Turn* node acts as a gating node in which its deadline is 64 times greater than the *RCS Mult* node, but the deadline values for the remaining nodes are the same as the *Corner Turn* node. Since $i > 0$ and $y_i \leq d_i < d_{i+1}$, $B_{BF}(Q_i)$ and $B_{DF}(Q_i)$ for the queue labeled *RCS* are evaluated with the same expression:

$$\begin{aligned}
B_{BF}(Q_4 = RCS) = B_{DF}(Q_4 = RCS) = B_{EDF}(Q_4 = RCS) &= (\lfloor \frac{d_{Corner\ Turn}}{y_{RCS\ Mult}} \rfloor \cdot x_{RCS\ Mult} \cdot p_{RCS}) + r_{RCS} \\
&= (\lfloor \frac{64 \cdot 3.6ms}{3.6ms} \rfloor \cdot 1 \cdot 256) + (256 \cdot 127) = (64 \cdot 256) + (256 \cdot 127) = 256 \cdot 191 = 48,896
\end{aligned}$$

By Theorem 7.3, the total buffer space required for the graph to execute with EDF or BF-EDF scheduling is less than or equal to 148,086 tokens. Since $d_{i+1} \neq d_i$, $\forall i$, Theorem 7.4 is not applicable.

By Theorem 7.6, the total buffer space required to execute the SAR graph with DF-EDF scheduling when $d_i = y_i$ is less than or equal to $\sum_{i=0}^{n-1} B_{DF}(Q_i) = 82,806$.

We have already established that Theorems 7.3, 7.4, and 7.6 are upper bounds on buffer needs for the graph, depending on deadline values and scheduling algorithms. For some graphs, these may even be least upper bounds. We show in the next section, however, that these are not tight bounds for the SAR graph.

7.5 Reducing Buffer Bounds Further

We are able to reduce the buffer bounds derived in §7.4 by taking advantage of specific attributes of the SAR graph and features of the scheduling algorithms. Since EDF scheduling does not specify how deadline ties are broken, we cannot reduce the buffer bounds from what we have already established for canonical EDF scheduling. We can, however, take advantage of the deterministic tie breaking algorithms of BF-EDF and DF-EDF to find lower buffer bounds. Since the first queue in the graph accepts data from an external device, we will always include its maximum buffer needs in our new bounds.

BF-EDF Scheduling with $\mathbf{d_i = y_0}$. Observe that for the SAR graph when the nodes after the *Corner Turn* node execute, the queue labeled *RCS* will only contain $256 \cdot 64$ tokens. Moreover, the queues labeled *Azimuth*, *AFFT*, and *Mult* can only contain tokens between the time the *Corner Turn* node executes and the next time the source node delivers data. Therefore, we can get by with $118 + 32,768 + 32,768 + (256 \cdot 64) = 82,038$ tokens.

Taking the analysis further and fully exploiting the properties of the SAR graph, we observe that when the *Azimuth FFT* node executes it appends 128 tokens to its output queue and then consumes 128 from its input queue. Thus the total number of tokens left on its input and output queues does not change, and the total number of tokens on the two queues at any one time is never more than 32,768 + 128. But when the *Azimuth FFT* node executes, the input queue to the *Corner Turn* node only contains 16,384 tokens. Therefore, we can actually reduce the buffer bound for BF-EDF scheduling of the SAR graph when $\forall i > 0 : d_i = y_0 = 3.6ms$ to $118 + 32,768 + 32,768 = 65,654$ tokens.

DF-EDF Scheduling with $\mathbf{d_i = y_0}$. Since $\forall i > 0 : d_i = y_0 = 3.6ms$, we can reduce the bound on the buffer requirements with DF-EDF scheduling even further by taking advantage of specific features of the SAR graph. Observe that when node *Window Data*, *Range FFT*, or *RCS Mult* executes its input queue contains at most 256 tokens, and it produces 256 tokens on its output queue before consuming the 256 tokens on the input queue. Therefore the queues labeled *Fill*, *Window*, and *RFFT* never contain more than (256 + 256) tokens between them at any one time. When they contain any tokens, the queues labeled *Azimuth*, *AFFT*, and *Mult* are empty, and this latter set of queues never contain more than $128 + (256 \cdot 128)$ tokens at one time. This maximum occurs during the 1^{st} execution of the *Azimuth FFT* node after the *Corner Turn* node produces $(256 \cdot 128)$ tokens, which means the queue labeled *RCS* contains $(256 \cdot 64)$ tokens when this

maximum occurs. Therefore, we can actually reduce the buffer bound for DF-EDF scheduling of the SAR graph when $\forall i > 0 : d_i = y_0 = 3.6ms$ to $118 + 32,768 + 32,768 = 65,654$ tokens.

BF-EDF Scheduling with $\mathbf{d_i = y_i}$. Now consider what happens to the buffer bounds when $\forall i > 0 : d_i = y_i$. By Theorem 7.3, the total buffer space required for the graph to execute with BF-EDF scheduling is less than or equal to 148,086 tokens. Observe that the queues labeled *Azimuth*, *AFFT*, and *Mult* can only contain tokens between executions of the *Corner Turn* node since they have the same deadline. Therefore, these three queues never contain more than a total of $(32,768 + 128)$ tokens. The queues labeled *Fill*, *Window*, *RFFT*, and *RCS* never contain more than $(256 + 48,896)$ tokens, but if these queues contain this many tokens then the queue labeled *Azimuth* must be empty. Whenever the queues labeled *Azimuth*, *AFFT*, or *Mult* contain tokens, the queue labeled *RCS* can hold at most $r_{RCS} = 32,512$ tokens. Hence, we can get by with space for $118 + 48,896 + 32,768 = 81,782$ tokens.

DF-EDF Scheduling with $\mathbf{d_i = y_i}$. By Theorem 7.6, the total buffer space required to execute the SAR graph with DF-EDF scheduling when $d_i = y_i$ is less than or equal to $\sum_{i=0}^{n-1} B_{DF}(Q_i) = 82,806$. For the SAR graph, we can reduce this bound further.

Setting $d_i = y_i$ implies $d_i = 3.6ms$ for nodes *Zero Fill*, *Window Data*, *Range FFT*, and *RCS Mult*. The rest of the nodes in the graph have $d_i = 64 \cdot 3.6ms$, and the *Corner Turn* node has a rate of $(1, 64 \cdot 3.6ms)$. Therefore, the buffer needs are maximized when the *Corner Turn* node accumulates as much data as possible before executing, which then enables 256 executions of each of the subsequent nodes in the chain. Let the release time of the *Corner Turn* node be $127 \cdot 3.6ms$. The deadline for this release is $(127 \cdot 3.6ms) + (64 \cdot 3.6ms) = 191 \cdot 3.6ms$. Observe that the 191^{st} release of the *Zero Fill* node occurs at time $190 \cdot 3.6ms$ (assuming the first release was at time 0), and the deadline for this release will be $191 \cdot 3.6ms$. With DF-EDF scheduling, the *Corner Turn* node will execute before this release of the *Zero Fill* node. Thus, at most $190 \cdot 256 = 48,640$ tokens can accumulate on the queue labeled *RCS* before the *Corner Turn* node executes, produces 32,768 tokens on its output queue (the queue labeled *Azimuth*), and consumes 16,384 tokens from its input queue (the queue labeled *RCS*). Since the data is produced on its output queue before data is consumed from the input queue, the total buffer space required when the *Corner Turn* node executes in the interval $(190 \cdot 3.6ms,\ 191 \cdot 3.6ms)$ is $48,640 + 32,768$ tokens. The 256 executions of each down stream node (i.e., the nodes *Azimuth FFT*, *Kernel Mult*, and *Azimuth IFFT*) will inherit the release release time $127 \cdot 3.6ms$ and be assigned deadlines of $191 \cdot 3.6ms$. Since these nodes are scheduled with DF-EDF, the buffer requirements are maximized during the 1^{st} execution of the *Azimuth FFT* node. This node will produce 128 tokens before it consumes 128 of the 32,768 tokens on its input queue. Hence, the maximum number of tokens on these queues is $32,768 + 128$ tokens, and this occurs when the queue labeled *RCS* contains 16,384 tokens. Putting all of this together, we see that, when $d_i = y_i$ and the SAR graph is scheduled with DF-EDF, the queues will contain at most $118 + 48,640 + 32,768 = 81,526$ tokens at any one time.

8 Summary

In most "real-time" dataflow methodologies, system engineers are unable to analyze the real-time properties of dataflow graphs like those created using PGM. We have shown that this is not an intrinsic property of the methodologies, and that by applying scheduling theory to a PGM graph, we can determine exact node execution rates, which are dictated by the input data rate and the dataflow attributes of the graph. We have also shown how to bound latency and buffer requirements for an implementation of the graph scheduled with the preemptive EDF algorithm (and variations thereof) under the RBE task model.

Given a graph, the only free parameters we have to affect the latency or buffer bounds of the application are deadlines. If the latency requirement of the application is less than the latency value from the strong synchrony hypothesis (i.e., $(F(N_0, N_n)-1)\cdot y_0$), then the given graph will never meet its latency requirement. If the latency requirement is greater than the strong synchrony hypothesis bound but less than the lower bound $(F(N_0, N_n)-1)\cdot y_0+\sum_{i=1}^{n} e_i$, changing deadlines will not help the graph meet its latency requirement; a faster CPU is required.

If the latency requirement is greater than this lower bound but less than the upper bound $(F(N_0, N_n)-1)\cdot y_0 + d_n$ (where $d_i < d_{i+1}, 1 \leq i < n$) then one can attempt to follow the procedures outlined in §6.4 to reduce latency to the desired bound. Should this technique fail, the system engineer may need to make cost trade-offs. For example, if the deadline assignment technique outlined in §6.4 failed to yield satisfactory latency bounds before the schedulability test returned a negative result, the system engineer can decide whether to use a faster processor, or add memory to increase buffering. It is clear that the first choice resolves the latency problem, assuming a fast enough CPU exists. It may not be clear, however, that adding memory can reduce latency. Suppose the deadlines have been reduced such that the first k nodes in the chain all have deadlines equal to their rate interval (i.e., $d_i = y_i, \forall i : 1 \leq i \leq k$) and the last $(n-k)$ nodes have deadline values of d_k, but the latency bound is still too high and lowering the deadline parameters for the last $(n-k)$ nodes yields a negative result from (5.6). We may be able to reduce the latency bound further by setting all of the deadline parameters to $LatencyRequirement - (F(N_0, N_n)-1)\cdot y_0$. This increases the buffer requirements of the first k nodes, but may produce enough *slack* in the schedule such that the graph is now schedulable even though the deadline parameters of the last $(n-k)$ nodes have been reduced to achieve the desired latency bound. Should the graph become schedulable with these new deadline parameters but require too much memory, the system engineer can make cost trade-offs: more memory, faster CPU, or relaxed requirements.

Since our driving application has the topology of a chain, for space consideration we have restricted our analysis to chains and note that the results presented in this paper can be extended to general PGM graphs.

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