CSCE 351
Operating System Kernels

Intel Architecture

Steve Goddard
goddard@cse.unl.edu

http://www.cse.unl.edu/~goddard/Courses/CSCE351

Basic Execution Environment

- Eight 32-bit Registers
- General-Purpose Registers
- Six 16-bit Registers
- Segment Registers
- EFLAGS Register
- EIP (Instruction Pointer Register)

*The address space can be flat or segmented.
Application Programming
Registers

Alternate General-Purpose
Register Names

<table>
<thead>
<tr>
<th>General-Purpose Registers</th>
<th>16-bit</th>
<th>32-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AH AL</td>
<td>AX EAX</td>
<td></td>
</tr>
<tr>
<td>BH BL</td>
<td>BX EBX</td>
<td></td>
</tr>
<tr>
<td>CH CL</td>
<td>CX ECX</td>
<td></td>
</tr>
<tr>
<td>DH DL</td>
<td>DX EDX</td>
<td></td>
</tr>
<tr>
<td>BP</td>
<td>EBP</td>
<td></td>
</tr>
<tr>
<td>SI</td>
<td>ESI</td>
<td></td>
</tr>
<tr>
<td>DI</td>
<td>EDI</td>
<td></td>
</tr>
<tr>
<td>SP</td>
<td>ESP</td>
<td></td>
</tr>
</tbody>
</table>
Three Memory Management Models

Flat Memory Model

- Linear Address
- Linear Address Space

Segmented Model

- Offset
- Logical Address
- Segment Selector
- Segments
- Linear Address Space
- Line Segment

Flat-Addressable Model

- Offset
- Logical Address
- Segment Selector

*The linear address space may be paginated when using the flat-addressable model.

Flat Memory Model

Segment Registers

- The segment selector is used to segment register pair to transform the logical address into the linear address space.
Segmented Memory Model

EFLAGS Register
Stack Structure

Stack on Near and Far Calls

Note: On a near or far return, parameters are released from the stack. The return address value in the EBP is changed to the RET instruction.
Protection Rings

Stack Switch on a Call to Different Privilege Level
Stack Usage on Interrupt Handling