

CSCE 230 Computer Organization

Spring 2004
Steve Goddard

Contact person: Byron Blunk

Final Project, Y86 option
(15% of your course grade)

Due: 9:00pm Friday, April 30

For this assignment you will be implementing a version of the Y86 processor as specified in your textbook. The goal is to have a fully functioning, pipelined processor that can execute Y86 code correctly.

You may work in teams of up to 3, but I would like you to send me (Byron Blunk) an e-mail with your group member names when you have decided. This project will require a fair amount of meeting time with me, so scheduling in advance is highly recommended.

You are welcome to use whatever methods you want to implement this processor, the only restriction is that it *must* be able to be programmed onto an Altera FPGA. I suggest doing your development using the Altera MaxPlus+II software that you have installed on your laptops.

You can break the creation of this processor down into 3 basic parts: The ALU, the Memory/Registers, and the rest of the stages. I recommend starting off creating an ALU, then building a processor around that. It may be easier to create a sequential processor and pipeline it later.

You will be evaluated on the basis of your processor design. The points breakdown will be as follows.

Style/Comments:	25%
Design:	50%
Correctness:	25%

To achieve full points on style/comments, your solution must be well documented. If you are using an HDL, make sure to include a comment for every file explaining what it does, and for any non-trivial functions a simple explanation. For graphical layouts, be sure that the connections are as clean as possible, lines overlapping minimally, etc.

For Design, you must be able to explain how your design implements the Y86 instruction set. Particularly compelling would be examples of the overall design, problems encountered, and anything else that demonstrates and understanding of the Y86 architecture.

For correctness, you must be able to demonstrate correction execution of a Y86 program of my choosing. This may involve memory accesses, ALU operations, branch predictions, or anything else. Your processor's results will be compared against the Y86 simulator. And finally, your result will be programmed onto an Altera board, to verify that the layout works and fits onto an actual FPGA.