

## CSCE 434/834, Fall 2010

### Homework 5 (Due November 10)

*Note:* Weights of problems are as indicated.

1. [10%] Problem 9.10 from the textbook.
2. [20%] Problem similar to 9.35 but for the carry function  $F = A(B+C) = BC$ . The input and output load remain as specified in the problem.
3. [20%] Sketch the implementations of the 4-input XOR function in the following circuit techniques:

- a) Static CMOS
- b) Combination of static CMOS and transmission gates
- c) Pseudo-nMOS
- d) dual-rail domino

4. [30%] For this problem, refer to the Micropipelines paper by I. Sutherland (you can download it from UNL Libraries, from their ACM Digital Library subscription).

(a) Referring to Fig. 10 (Control circuit for micropipeline), assume there are  $n$ -stages in the pipeline. The state of the control circuit at any time can be represented by the combined states of the Muller C-elements. Precisely specify the patterns of circuit states that are possible for each of the following conditions of the pipeline, providing a sufficient justification for your answer:

1. Empty pipeline
2. Full pipeline
3. Pipeline with  $m$  ( $<n$ ) elements

(b) A complete state-diagram description of the Muller C element can be given by considering the total state (represented by  $\langle$ internal state, input state $\rangle$ ) of the circuit as nodes and input transitions causing appropriate transitions between nodes.

1. Provide a state-diagram description for the 2-input Muller C element.
2. Provide a state-diagram description for the 3-input Muller C element and then sketch the generalization to  $n$ -input Muller C element.

(c) Fig. 9 shows five other logic modules for events, namely (1) XOR, (2) TOGGLE, (3) SELECT, (4) CALL, (5) ARBITER.

1. Choose one of the first three modules according to the number:  $\langle$ last digit of your UNL ID number modulo 3 + 1 $\rangle$  and obtain a dynamic or static CMOS implementation of the same, comparable to Figures 6 or 7 for the Muller C element. Provide arguments for the correctness of your design.
2. Sketch out possible CMOS implementations for CALL and ARBITER.

5. [20%] Problem 10.10 from the textbook